

# High-Precision, Programmable 1-10MHz Bandwidth, 0-20dB Gain Communication Channel for Digital Video Applications

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## Abstract

The analog signal processing portion of a digital video demodulation scheme is built in a 5V BiCMOS process. The channel is both cutoff frequency and gain programmable from 1→10 MHz and 0→20dB, respectively. The filter is realized as a 4<sup>th</sup> order Gm/C Butterworth lowpass and includes in-package trim for accurate control. A programmable gain amplifier is placed in front of the filter for better S/N performance (>40dB) and lower intermodulation distortion (>-52dB). The PSRR of this single-ended channel is better than 40dB. The channel dissipates 250mW.

## 1. Introduction

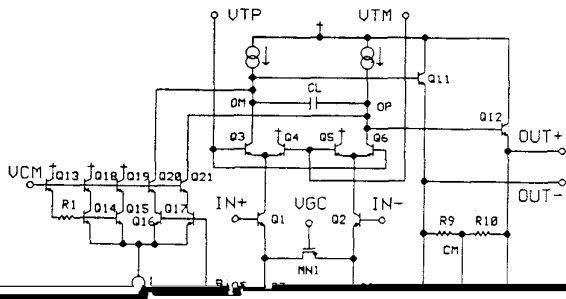
Digitally encoded video signals can be transmitted using either MCPC (multiple channel per carrier) mode, where all channel data are multiplexed and transmitted on a single carrier, or SCPC (single channel per carrier) mode, which allows each channel to be transmitted on its own subcarrier. Since both SCPC and MCPC modes utilize different carrier frequencies and different modulation techniques, the cutoff and gain requirements for the channel must vary, with the variation occurring as lower gain for higher cutoff and higher gain for lower cutoff. A practical digital video receiver is shown in Fig. 1. The system consists of an RF preamp, two mixers, a quadrature local oscillator (LO), two programmable, continuous-time filters, two ADCs, and a demodulator. After down-conversion, the quadrature data

schemes. The accuracy (less than 5% for the cutoff and 1dB for the gain) is required for acceptable bit-error-rate (BER). A monolithic realization of a data filter channel, where both the cutoff and gain can be programmed over a 10X range, is presented in the following. It should be noted that wide programmability combined with the need for accurate control, plus the requirements for low channel noise and intermodulation distortion, produce a challenging set of design constraints for the data channel.

## 2. Channel Overview

The block diagram of the data filter channel appears in Fig. 2. It consists of a single-to-differential converter (S/D), a programmable gain amplifier (PGA), widely-programmable continuous-time lowpass filter, a fixed gain amplifier (FGA) and a differential-to-single-ended converter (D/S). This configuration results in superior signal-to-noise (S/N) performance (over 12dB improvement) as compared to an arrangement where the placement of the PGA and FGA are reversed. The external ac coupling capacitors eliminate any dc voltage offsets between the two phases of the differential signal. This is essential for good distortion performance through the D/S circuit. The single-ended I/O complicated the design and results in some degradation in distortion and power-supply rejection ratio (PSRR) performance.

The chip is built in a 7 GHz, 0.8 μm BiCMOS process. The use of a high-performance process was necessitated by the requirement that the frequency response, out to 2X the



operation, so it exhibits excellent high frequency response (GBW > 50 MHz). The load capacitor,  $C_L$ , can be split into two capacitors to ground, which will provide increased phase margin in the feedback loop.

#### 4. Filter Tuning/Programming

##### A. MOS $g_{ds}$ Tuning

The triode region MOS device in the transconductor

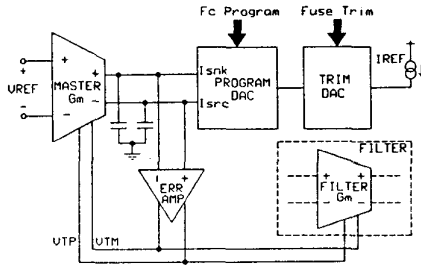


Fig. 5. GM stage tuning and programming circuit.

independent reference current that is applied to a tuning loop for the  $G_M$  stage. The control loop, shown in Fig. 5, corrects for any temperature variations. For cutoff frequency programming, a DAC is used to modify the trimmed reference current prior to the tuning loop.

The tuning loop consists of a differential reference current (modified by the Trim and Program DACs), a master  $G_M$  stage with a differential temperature-independent voltage reference as its input, an error amplifier, and compensation capacitors. The error amp adjusts the current splitting pairs in the master  $G_M$  stage until its output current is equal to the modified reference current. The  $g_m$  of the master  $G_M$  cell is

$$g_m = \frac{I_{REF}^*}{V_{REF}} \quad (2)$$

where  $I_{REF}^*$  is the trimmed and programmed reference current. The differential control voltages, VTP and VTM, are also applied to all the  $G_M$  cells in the filter and since the master  $G_M$  cell is a replica of the filter  $G_M$  stages, their transconductances are all equal.

### 5. S/D, Programmable Gain Amp, & D/S

Consider the amplifier shown in Fig. 6, which is a BiCMOS, folded-cascode version of (3). It combines the S/D with the PGA, resulting in lower power, smaller area, reduced distortion and noise levels, and a wider frequency response. Its linearity is enhanced by the two operational transconductance amplifiers (OTAs) that increase the effective  $g_m$  of  $Q_1$  and  $Q_2$  by the voltage gain of the OTA, so that  $R_1$  appears to be driven from a nearly ideal voltage source. Current-splitting pairs were again chosen for gain control. The PGA gain can be approximated as

$$\begin{aligned} A_v &\approx \frac{R_2}{R_1} \frac{1}{1 + \exp\left(\frac{V_2 - V_1}{V_T}\right)} \approx \frac{R_2}{R_1} \exp\left(\frac{V_1 - V_2}{V_T}\right) \\ &= \frac{R_2}{R_1} \exp\left(\frac{I_{prg} R_4}{V_T}\right) = \frac{R_2}{R_1} \exp\left(\frac{m R_4}{R_3}\right) \end{aligned} \quad (3)$$

where  $\exp((V_2 - V_1)/V_T) \gg 1$  is assumed.  $R_3$  and  $R_4$  are on-chip resistors,  $R_2 = R_9 + R_{10}$ , and  $I_{prg} = mV_T/R_3$ .  $I_{prg}$  is a PTAT current controlled by a linear DAC that provides for temperature independent gain control in linear dBs.

In order to minimize response inaccuracies in the filter transfer function, the PGA is designed for a bandwidth of over 200 MHz. The folded cascode design provides for high frequency performance, as well as high output impedance ( $r_o \gg R_2$ ) which reduces gain errors. Finally, the dc level of the output is controlled by a CMF loop which is necessary to minimize any dc input variation to the filter that would result in a channel gain error.

As with the S/D and PGA, the FGA and D/S functions were combined into one block. The FGA is similar in design to the PGA. However, both the current splitting pairs and the CMF loop are absent. The output buffer is a simple emitter follower stage.

### 6. Measured Results

A partial die photo showing both I and Q data filter channels and their associated tuning circuitry appears in Fig. 7. It can be seen that the tuning and programming circuitry occupies approximately the same area as the filter. This overhead in area was justified by the tight accuracy and wide programmability requirements.

The performance results are summarized in Table 1. Fig. 8 shows the amplitude response of the channel for the extremes, 1MHz cutoff with 20dB of gain and 10MHz cutoff with 0dB of gain. Fig. 9 shows the difference between the actual amplitude response of the channel and an ideal Butterworth filter at 10MHz. Deviations from ideality are believed to be due to inexact cancellation of parasitic zeros and low dc gain in the  $G_M$  stage at the higher and lower cutoff frequencies, respectively. The data channel THD for the 10MHz-0dB case is shown in Fig. 10 for an input at 2MHz and 300mV<sub>p-p</sub>. The even order harmonics are created during the differential to single-ended conversion process.

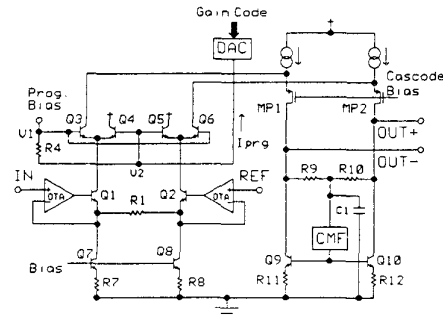


Fig. 6. Highly-linear programmable gain amplifier.

## 6.1.3

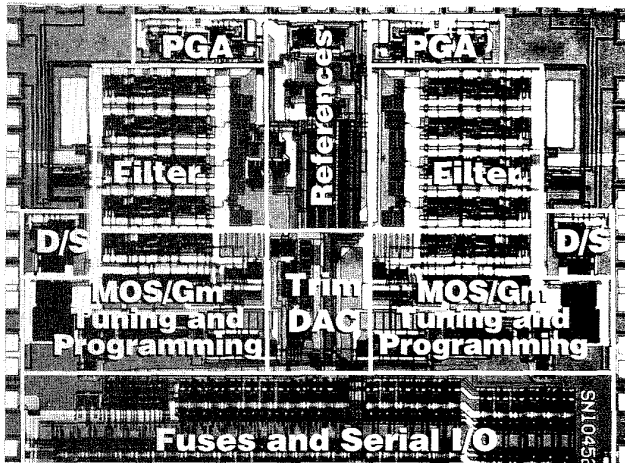


Fig. 7. Die photo showing I/Q channels and tuning circuitry.

Table 1  
Performance Results

Cutoff Frequency	1-10 MHz
Channel Gain	0-20 dB
Initial Cutoff Accuracy	< 2 %
Cutoff Variation (0-70 ° C)	< 3 %
Amplitude Response Accuracy (dc to $f_c$ )	< 0.25 dB
I-Q Cutoff Matching	< 2 %
I-Q Gain Matching	< 1 dB
THD ( $V_{out} = 300mV$ )	< 0.4 %
IMD ( $f_c=1MHz$ , $A_v=20dB$ , $f_{in} = 9 \& 10MHz @ 25mV$ ea.)	< 0.25 %
Output Noise (integrated to 100MHz)	< 300 $\mu V_{rms}$
PSRR (to 1 MHz)	> 40 dB

## 7. Conclusions

A dual, programmable cutoff frequency and gain data channel has been presented that offers precise control over a 10X range for both cutoff frequency and gain. Circuits were shown that allow the channel to maintain an approximately ideal 4<sup>th</sup> order Butterworth response while

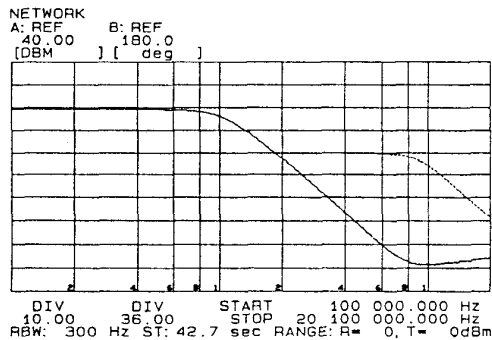


Fig. 8. Amplitude response of the data filter channel.

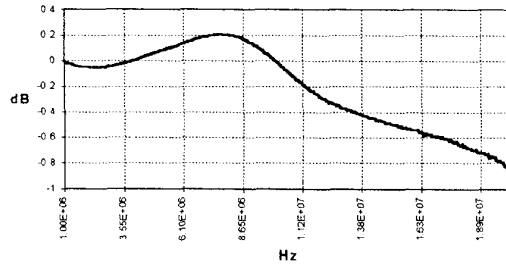


Fig. 9. Channel response accuracy to ideal 4<sup>th</sup> order Butterworth.

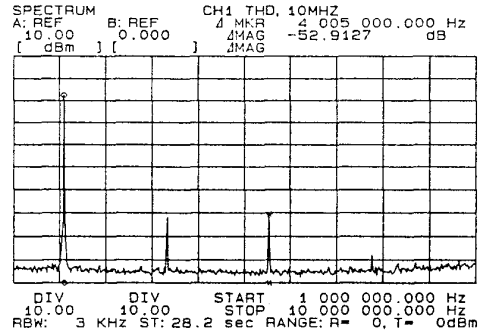


Fig. 10. Data filter channel THD for  $f_c = 10MHz$ .

accurately controlling the bandwidth from 1 to 10 MHz. Though the I/O of the channel is single-ended, the levels of intermodulation distortion, THD and PSRR were shown to be moderately low. An overview of the digital video application, as well as the factors that drive the need for such an accurate, programmable channel, were discussed.

## Acknowledgments

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