High-Precision, Programmable 1-10MHz Bandwidth, 0-20dB Gain Communication Channel for Digital Video Applications

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Abstract

The analog signal processing portion of a digital video demodulation scheme is built in a 5V BiCMOS process. The channel is both cutoff frequency and gain programmable from 1→10 MHz and 0→20dB, respectively. The filter is realized as a 4^{th} order Gm/C Butterworth lowpass and includes in-package trim for accurate control. A programmable gain amplifier is placed in front of the filter for better S/N performance (>40dB) and lower intermodulation distortion (>-52dB). The PSRR of this single-ended channel is better than 40dB. The channel dissipates 250mW.

1. Introduction

Digitally encoded video signals can be transmitted using either MCPC (multiple channel per carrier) mode, where all channel data are multiplexed and transmitted on a single carrier, or SCPC (single channel per carrier) mode, which allows each channel to be transmitted on its own subcarrier. Since both SCPC and MCPC modes utilize different carrier frequencies and different modulation techniques, the cutoff and gain requirements for the channel must vary, with the variation occurring as lower gain for higher cutoff and higher gain for lower cutoff. A practical digital video receiver is shown in Fig. 1. The system consists of an RF preamp, two mixers, a quadrature local oscillator (LO), two programmable, continuous-time filters, two ADCs, and a demodulator. After down-conversion, the quadrature data signals are filtered, amplified, and converted to digital form. The wide programmability of the data channel filter is mandatory due to the variety of data rates and modulation schemes. The accuracy (less than 5% for the cutoff and 1dB for the gain) is required for acceptable bit-error-rate (BER). A monolithic realization of a data filter channel, where both the cutoff and gain can be programmed over a 10X range, is presented in the following. It should be noted that wide programmability combined with the need for accurate control, plus the requirements for low channel noise and intermodulation distortion, produce a challenging set of design constraints for the data channel.

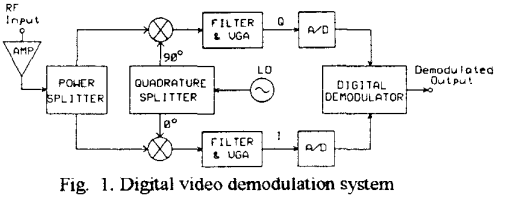

Fig. 1. Digital video demodulation system

2. Channel Overview

The block diagram of the data filter channel appears in Fig. 2. It consists of a single-to-differential converter (S/D), a programmable gain amplifier (PGA), widely-programmable continuous-time lowpass filter, a fixed gain amplifier (FGA) and a differential-to-single-ended converter (D/S). This configuration results in superior signal-to-noise (S/N) performance (over 12dB improvement) as compared to an arrangement where the placement of the PGA and FGA are reversed. The external ac coupling capacitors eliminate any dc voltage offsets between the two phases of the differential signal. This is essential for good distortion performance through the D/S circuit. The single-ended I/O complicated the design and results in some degradation in distortion and power-supply rejection ratio (PSRR) performance.

The chip is built in a 7 GHz , 0.8 μm BiCMOS process. The use of a high-performance process was necessitated by the requirement that the frequency response, out to 2X the cutoff frequency, should be nearly ideal. This dictated that all circuits in the signal path must be very wideband.

3. Programmable Filter

The Butterworth transfer function is chosen for its

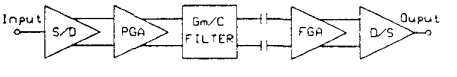

Fig. 2. Analog processing data filter channel.

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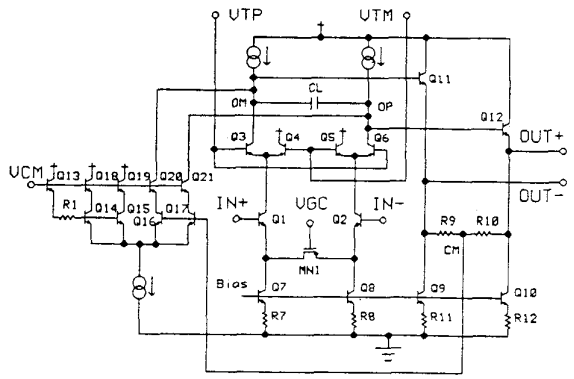

Fig. 3. Widely tunable transconductance stage.

maximally-flat passband magnitude response. Sufficient attenuation is achieved from a 4th order filter using g_m-C techniques and composed of two cascaded biquad sections. A main design issue in the filter is the wide programming range of 1 to 10 MHz. This requires a transconductor (G_M) whose gm can be varied > 18X to compensate for capacitor variations and to allow further minimization of BER by dynamically modifying the cutoff frequency as needed.

A realization of a widely-tunable transconductor is shown in Fig. 3. It consists of a bipolar differential pair, Q_1 and Q_2, degenerated by a triode region MOS device, MN_1. For $g_{mQ1} >> g_{ds1}$, the transconductance of the input stage is $g_m \approx g_{ds1}$. The wide tunability is achieved by the current splitting pairs Q_3-Q_4 and Q_5-Q_6, which were chosen over a Gilbert cell for their lower noise and higher output impedance. Dual-input G_M stages were obtained by duplicating Q_1,Q_2, and MN_1 and their associated current sources. The different g_m/C of each integrator was achieved with equal transconductance among all G_M stages and ratioed capacitors. The worst case phase error of any integrator is < 0.75° at its unity-gain frequency.

Since the g_m of the input stage is the g_{ds} of MN_1, it is heavily dependent upon the common-mode (c-m) level of the input. This fact drives the need for a very good common-mode feedback (CMF) loop that can keep variations in the c-m voltage to less than 10mV if the cutoff and gain accuracies are to be preserved. The CMF loop consists of transistors Q_{13}-Q_{21} in Fig. 3 in a cascoded, dual-differential pair arrangement. If the detected output c-m level, CM, rises above(or falls below) the reference c-m voltage, VCM, minus 1 V_{BE}, then Q_{16} and Q_{17} will draw more (or less) current from nodes OP and OM, thus stabilizing the output c-m voltage at OP and OM to be equal to VCM. The cascode devices, Q_{20} and Q_{21}, increase the output impedance of the CMF loop so that it will not degrade the transconductor's output impedance. The CMF loop contains a single gain stage and employs current-mode operation, so it exhibits excellent high frequency response (GBW > 50 MHz). The load capacitor, C_L, can be split into two capacitors to ground, which will provide increased phase margin in the feedback loop.

4. Filter Tuning/Programming

A. MOS g_{ds} Tuning

The triode region MOS device in the transconductor replaces a laser-trimmed resistor used in (1). Previously, in (2) , to compensate for process and temperature variations in g_{ds}, a PLL was used to control the MOS gate voltage, VGC. A significantly more compact circuit that performs the MOS g_{ds} tuning appears in Fig. 4. This circuit combines a replica of a G_M input stage with an 'error amplifier' to control VGC. A bandgap-derived voltage reference that is differential about the input c-m voltage is applied to the replica input stage so that MN_1 is biased as it is in the G_M stage. A temperature-independent reference current is sourced into the drain of the MN_1. This forces the current in Q_2, and consequently MP_2, MP_1 and Q_1, to I_B - I_{REF2}. However, to satisfy KCL at the MOSFET drain, VGC is adjusted until $I_{REF2}/2$ flows through MN_1. At that point the r_{ds} of the MOSFET is given by

$$r_{ds} = \frac{V_{REF}}{\left(I_{REF2}/2\right)}. \qquad (1)$$

The PMOS current mirror acts as an error amplifier by forcing the same current through Q_1 and Q_2. VGC is then applied to all MOSFET 'resistors' in all G_M stages.

B. G_M Tuning

With the MOSFET tuned to a specific resistance, the G_M stage must be adjusted for capacitance variations. A quasi-open loop approach was chosen, where fuse trimming is performed during in-package testing to adjust the cutoff frequency to a precise value. The capacitor process variation is trimmed by adjusting a temperature-

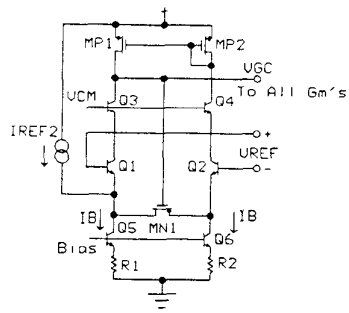

Fig. 4. MOSFET g_{ds} tuning circuit.

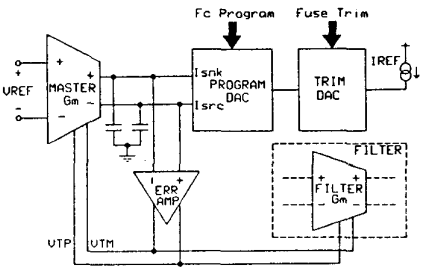

Fig. 5. GM stage tuning and programming circuit.

independent reference current that is applied to a tuning loop for the G_M stage. The control loop, shown in Fig. 5, corrects for any temperature variations. For cutoff frequency programming, a DAC is used to modify the trimmed reference current prior to the tuning loop.

The tuning loop consists of a differential reference current (modified by the Trim and Program DACs), a master G_M stage with a differential temperature-independent voltage reference as its input, an error amplifier, and compensation capacitors. The error amp adjusts the current splitting pairs in the master G_M stage until its output current is equal to the modified reference current. The gm of the master G_M cell is

$$gm = I^*_{REF} / V_{REF} \tag{2}$$

where I^*_{REF} is the trimmed and programmed reference current. The differential control voltages, VTP and VTM, are also applied to all the G_M cells in the filter and since the master G_M cell is a replica of the filter G_M stages, their transconductances are all equal.

5. S/D, Programmable Gain Amp, & D/S

Consider the amplifier shown in Fig. 6, which is a BiCMOS, folded-cascode version of (3). It combines the S/D with the PGA, resulting in lower power, smaller area, reduced distortion and noise levels, and a wider frequency response. Its linearity is enhanced by the two operational transconductance amplifiers (OTAs) that increase the effective g_m of Q_1 and Q_2 by the voltage gain of the OTA, so that R_1 appears to be driven from a nearly ideal voltage source. Current-splitting pairs were again chosen for gain control. The PGA gain can be approximated as

$$Av \approx \frac{R_2}{R_1}\frac{1}{1+\exp\left(\frac{V_2-V_1}{V_T}\right)} \approx \frac{R_2}{R_1}\exp\left(\frac{V_1-V_2}{V_T}\right)$$

$$= \frac{R_2}{R_1}\exp\left(\frac{I_{prg}R_4}{V_T}\right) = \frac{R_2}{R_1}\exp\left(\frac{mR_4}{R_3}\right) \tag{3}$$

where $\exp((V_2-V_1)/V_T) >> 1$ is assumed, R_3 and R_4 are on-chip resistors, $R_2 = R_9+R_{10}$, and $I_{prg} = mV_T/R_3$. I_{prg} is a PTAT current controlled by a linear DAC that provides for temperature independent gain control in linear dBs.

In order to minimize response inaccuracies in the filter transfer function, the PGA is designed for a bandwidth of over 200 MHz. The folded cascode design provides for high frequency performance, as well as high output impedance ($r_o >> R_2$) which reduces gain errors. Finally, the dc level of the output is controlled by a CMF loop which is necessary to minimize any dc input variation to the filter that would result in a channel gain error.

As with the S/D and PGA, the FGA and D/S functions were combined into one block. The FGA is similar in design to the PGA. However, both the current splitting pairs and the CMF loop are absent. The output buffer is a simple emitter follower stage.

6. Measured Results

A partial die photo showing both I and Q data filter channels and their associated tuning circuitry appears in Fig. 7. It can be seen that the tuning and programming circuitry occupies approximately the same area as the filter. This overhead in area was justified by the tight accuracy and wide programmability requirements.

The performance results are summarized in Table 1. Fig. 8 shows the amplitude response of the channel for the extremes, 1MHz cutoff with 20dB of gain and 10MHz cutoff with 0dB of gain. Fig. 9 shows the difference between the actual amplitude response of the channel and an ideal Butterworth filter at 10MHz. Deviations from ideality are believed to be due to inexact cancellation of parasitic zeros and low dc gain in the G_M stage at the higher and lower cutoff frequencies, respectively. The data channel THD for the 10MHz-0dB case is shown in Fig. 10 for an input at 2MHz and 300mV$_{p-p}$. The even order harmonics are created during the differential to single-ended conversion process.

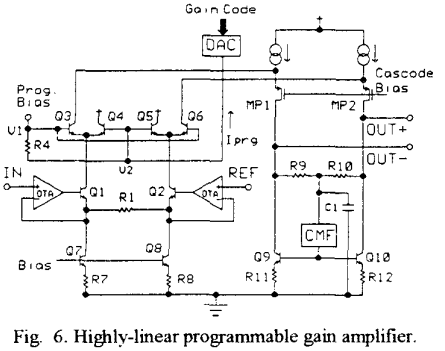

Fig. 6. Highly-linear programmable gain amplifier.

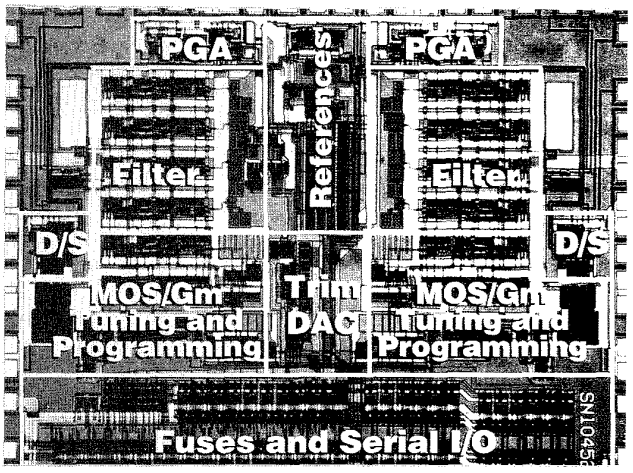

Fig. 7. Die photo showing I/Q channels and tuning circuitry.

Table 1
Performance Results

Cutoff Frequency	1-10 MHz
Channel Gain	0-20 dB
Initial Cutoff Accuracy	< 2 %
Cutoff Variation (0-70 ° C)	< 3%
Amplitude Response Accuracy (dc to f_c)	< 0.25 dB
I-Q Cutoff Matching	< 2 %
I-Q Gain Matching	< 1 dB
THD (Vout = 300mV)	< 0.4 %
IMD (fc=1MHz, A_v=20dB, fin = 9 & 10MHz @ 25mV ea.)	< 0.25 %
Output Noise (integrated to 100MHz)	< 300 μVrms
PSRR (to 1 MHz)	> 40 dB

7. Conclusions

A dual, programmable cutoff frequency and gain data channel has been presented that offers precise control over a 10X range for both cutoff frequency and gain. Circuits were shown that allow the channel to maintain an approximately ideal 4th order Butterworth response while accurately controlling the bandwidth from 1 to 10 MHz. Though the I/O of the channel is single-ended, the levels of intermodulation distortion, THD and PSRR were shown to be moderately low. An overview of the digital video application, as well as the factors that drive the need for such an accurate, programmable channel, were discussed.

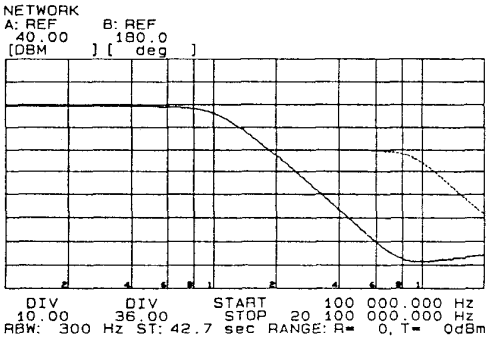

Fig. 8. Amplitude response of the data filter channel.

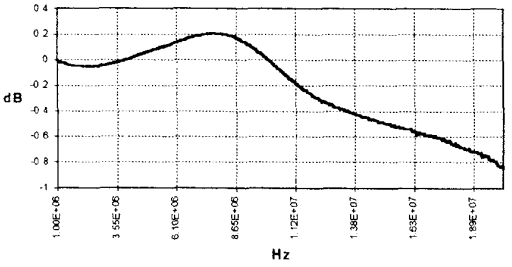

Fig. 9. Channel response accuracy to ideal 4th order Butterworth.

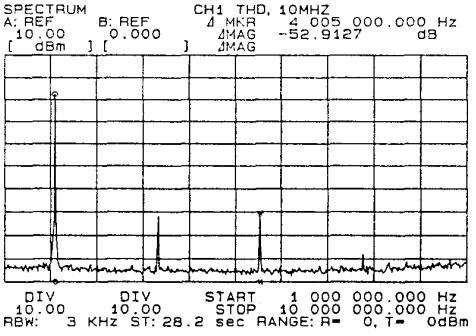

Fig. 10. Data filter channel THD for fc = 10MHz.

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