ON AUTOMATION PLACEMENT AND ROUTING OF GATE ARRAY

A.Wyszyński, R.Kubiak
Institute of Electron Technology, 02-668 Warszawa
Al.Lotników 38/46 POLAND

A method of fully automatic placement and routing of Gate Array is presented. The constructive placement is combined with tracing the connections. Next, the channel router generates the final routing, optimizing the number of layer changes and crossings. The results of the presented method's implementation are included.

1. INTRODUCTION

The paper presents a CAD method of bipolar Gate Array design. The array consist of regulary placed, quasi-aquare cells with horizontal and vertical channels for leading the connections between them /see Fig. 1/.

Two layers for connections are permitted. The layout design has two steps :
- Simultaneous placement and initial tracing of connections.
- Final routing, defining the geometry of connections and partitioning of two metalization layers.

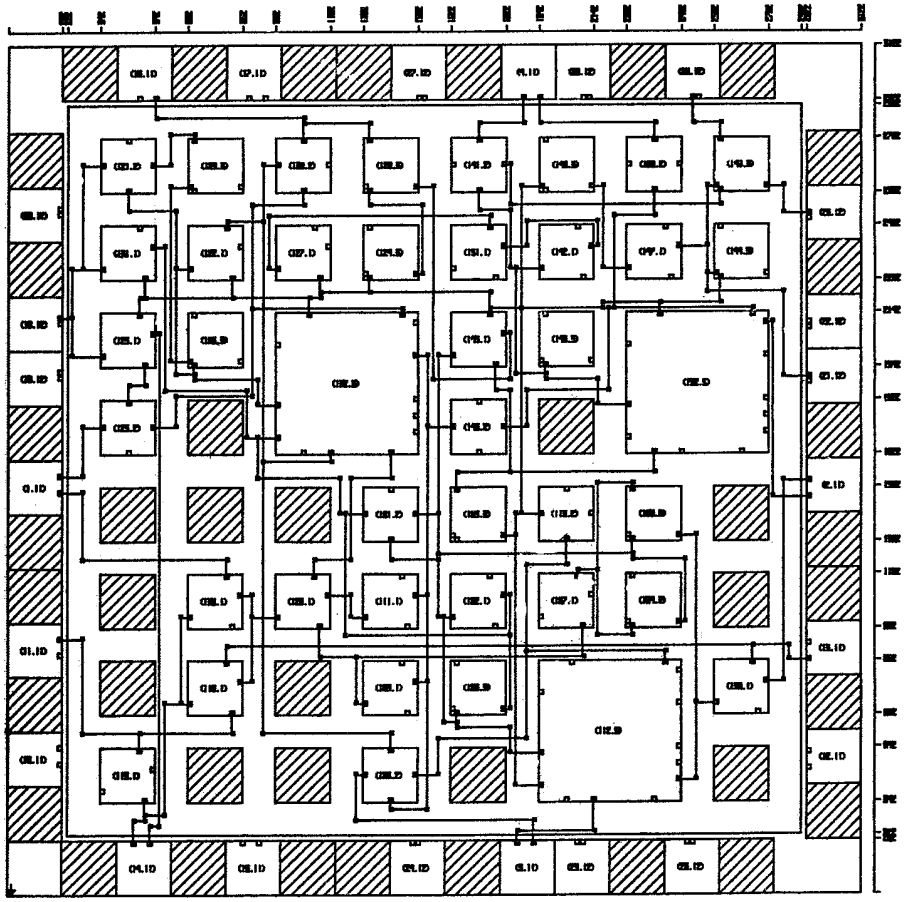

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Fig.1 The test Gate Array layout drawing from a plotter. The Gate Array contains 64 cells and 52 bounding pads. Regulary placed cells arrange vertical and horizontal channels for leading connections. Supply and ground tracks are not plotted.

The placement is based on building up the array "cell by cell". Subsequently, the sets of unplaced cells and available places in the array are searched. Unoccupied cells laid in the neighbourhoods of the cells, which have already been placed, make the set of available places. Search is made for cells which have the greatest number of contacts not yet connected. A cell and a place are chosen on the basis of the minimum value of the target-function. The processed cell is solidly fixed in the chosen place of the array. Simultaneously, the tracks of connections to the placed cells are made. These tracks will form the data base for the final routing step.

The final routing starts when all cells are placed. Connections paths of each channel of array are projected separately. Channels can be projected in any order. Sequence of tracks in the chosen channel is analysed as first. By "sequence", it is understood the transversal order of tracks, from one edge of channel to the other. Then the sequence is chosen which gives minimal parasitic couplings between signal paths and minimises the number of layer changes, while preserving previous sequence, the exact connections paths, based on geometry rules, are established.

If the connections path goes through more then one channel, the path is projected partially. This fragment of the path only is designed, which is included in the considered channel. Process of designing is repeated for each channel of array in sequence.

As a result, coordinates of each segment of metalization with specified number of layer are obtained.

2. THE METHOD OF AUTOMATIC PLACEMENT AND TRACING THE CONNECTIONS

2.1. Principles

In order to build placing and tracing algorithms, following principles were established:

- the arrays dimensions are known and total number of cells is greater than the number of cells for placing,
- the cells are square or rectangular with sides in proportion close to 1,
- the cells orientation is fixed,
- single cell or rectangular block of cells can be placed,
- the bonding pads are regulary placed on 4 arrays sides,
- the channel width is given,
- the connections are led in two metalization layers,
- the connections are led in channels only, the areas of cells or blocks of cells are forbiden for outside connections,
- the ground and supply tracks are hand-designed and their shapes are not changed in the routing step.

2.2. Placing with the simultaneous tracing of the connections algorithm.

The algorithm creates the placing which is close to the optimum one. It is not optimum as a result of the limited number of checkings. In spite of this limitation, the placement still keeps proper quality.

The algorithm belongs to the group of constructive algorithms, the final result is obtained by adding successive cells to the group of cells already placed.

Target-function is the criterion of choosing a cell for placing. This function is based on the connection length between a cell to be placed and the one already located /see Fig. 2./. The location of a new call is found as follows; a set of placed cells with unrouted connections is created and searched. Neighbourhood of cell /see Fig. 3./ with many unrouted connections is searched first. There is the highest probability of finding appropiate place for cell location.

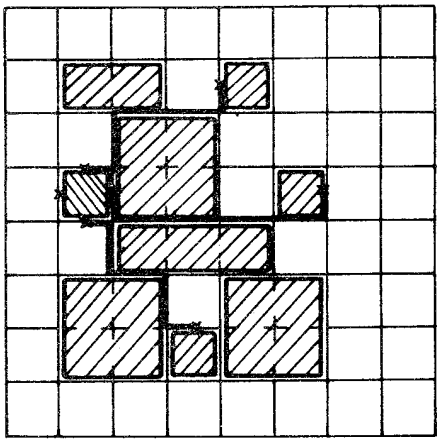

Fig. 2 The placing of single cell with tracing the connections to the cells or blocks of cells have already been placed.

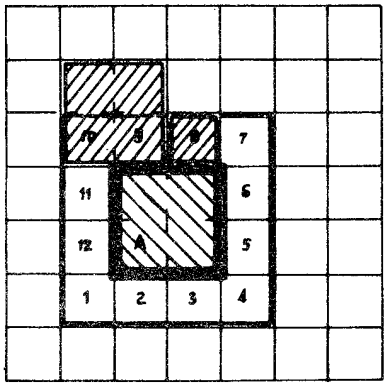

Fig. 3 Neighbourhood of block of cells A The cells with numbers 8,9,10 are occupied.

In order to simplify the placing program the date representation of cells and channels is transformed /see Fig. 4/.

2.3. Time relations of the placing algorithm.

Let us assume that n identical cells are to be placed and each locating requires the same number of operations. Each cell has the neighbourhood consisting of 8 cells. The number of operations N, for the k-th placement step would be described by following inequality:

$$N(k) \leq 8\,(n-k)$$

The total number of operations is the sum:

$$N_t = \sum_{k=1}^{n} N(k) \leq 8 \sum_{k=1}^{n} (n-k) =$$

$$= 8\left(\sum_{k=1}^{n} n - \sum_{k=1}^{n} k\right) = 8\left(n^2 - \frac{n(n+1)}{2}\right)$$

finally:

$$N_t \sim n^2$$

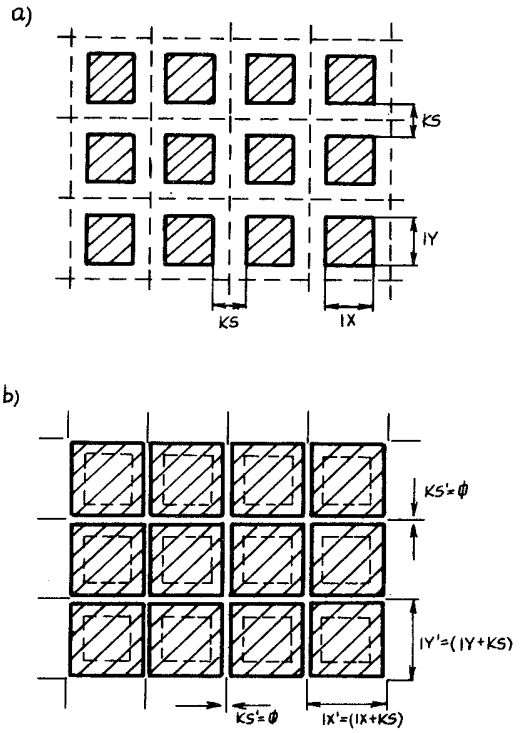

Fig. 4 Placing the cells with dimensions IX×IY separated by the channels with width KS /Fig. 4a/ is replaced by placing the cells with dimensions (IX+KS)×(IY+KS) separated by the channels with width equal zero. /Fig. 4b/.

3. THE FINAL ROUTING ALGORITHM

3.1. Principles

The purpose of this part of designing is to establish precise paths of metalization. The net connecting cells and blocks of cells is projected only. The connections inside cells and blocks are given.

Correctly designed connections must fulfil the following demands:
- The resistance of connections ought to be as low as possible. This is achieved by minimizing total connections length and number of vias /metalization layer changes/.
- Parasitic coupling between signal paths ought to be as low as possible. This is achieved by minimizing the number of paths' crossings and by increasing distances between paths.
- The obtained paths of connections must not effect on decrease production gain. This depends fully on the first two demands and minimum number of paths turnings.

3.2. The simplifications of the problem.

It is very difficult to obtain solution with the best electrical parameters of I.C. and with the highest production gain. The main problems to overcome are: defining precise algorithm's target function /many significant factors/ and time computing limitation. However in reality a "feasible" rather then an optimum solution is searched. It is possible to resolve this problem simplifying the target-function by taking into account the most powerful parameters only. So simplified algorithm gives nonoptimum results but by proper target-function choosing, the results can be acceptable by the designer.

To simplify the problem, it has been assumed that:
- Vertical and horizontal segments of paths are permitted only. The extension of the length of connections caused by this assumtion will be small due to specific gate array shape.
- Paths going transversely to supply and ground lines are placed on the first metalization layer, paths going along them are placed on the second layer. Supply and ground tracks by definition are placed on the second layer, paths crossing them must run on the opposite layer.
- The placement of paths in channel are quantified with module equal to minimal distance between two parallel paths /technological restriction/. There are no free positions for paths, they could be located in strictly defined places called lines /see Fig. 5/. The paths of connections in logical circuits have usually constant width, so this limitation has small influence on design results.
- Each channel of gate array is designed separately. This simplification is most powerful and it influences the paths' intersection number, but it allows considerably less complicated algorithm and speeds up its action.

3.3 The features of the algorithm.

With the above assumptions, metalization design brings on to assign segments of paths to earlier defined lines in channel /as a result of 3-th principle/.

Metalizations path length is determinated by distance between a chosen line and connections pins /see Fig. 6/. The number of paths crossing is determined by sequence of a chosen line in relation to other paths line /see Fig. 7/.

It should be pointed out that the channels in which the paths of connections go, are determined by placing algorithm. Final routing algorithm has no possibility to change them, it generates proper paths shape only. The routing algorithm has little impact on the length of paths but it is general on the interestion of paths. So the primary goal of tracing is to determine optimum sequence of the path of connections in channels, which minimize the number of paths crossings.

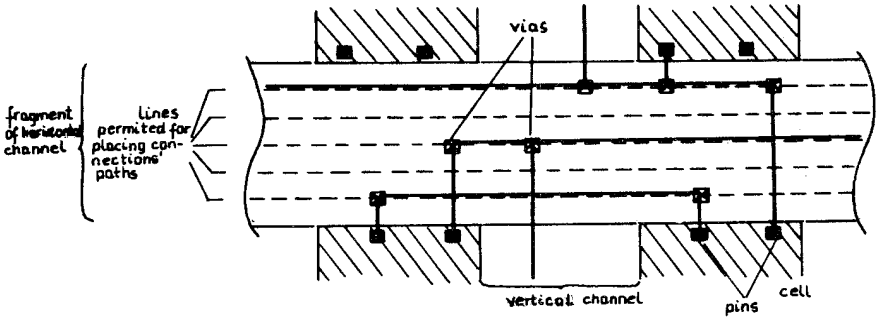

Fig. 5 Enlargement of channel's fragment. By dots are designed axises of connestions' paths.

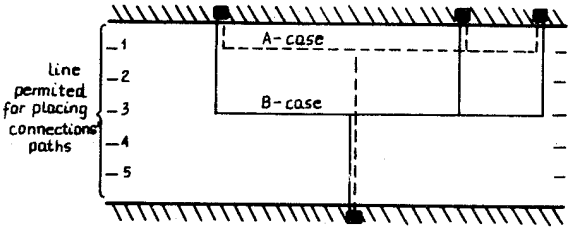

Fig. 6 Connection's path length is determinated by distance between chosen line and connection's pins. In A-case /chosen line no. 1/ the total length is lower than in B-case /chosen line no. 3/.

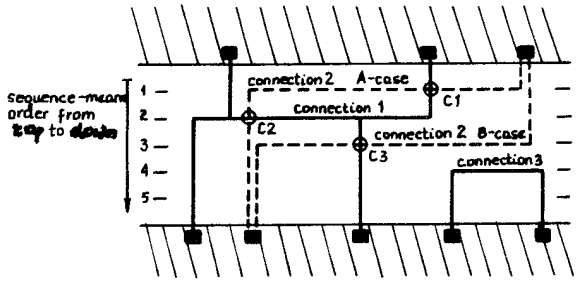

Fig. 7 Number of path crossing is determinated by sequence of chosen line in relation to other paths'lines. For connection no. 1 there are two orders /from top to down / :
A-case, sequence 2-1, crossings C1 and C2,
B-case, sequence 1-2, crossing C3.

This sequence is established at first for the given channel. In the next step, rectilinear segments of paths are placed on lines of channels preserving the previous sequence. If the segment of path could be located on one of several lines, this line is chosen, which assures the lowest path length.

4. FINAL RESULTS

The system based on the principles of the presented method is called "MATRIX". It has been programmed in FORTRAN IV and implemented on ODRA 1305 /ICL 1900/ computer under GEORGE-3 control. The system is fully automatic. The user can interact between programs only. If not satisfied he can overwrite some parameters for next step. There is no graphical interaction.

The final results of the system are as follows:
- the array's drawing with an exact design of metalization paths,
- the data file describing the metal mask of array. This file is used for Pattern Generator control.

The system consists of 5 programs and occupied the memory of maximum 48 K 24 bits words,

The "placement" part of system consists of 2 programs:
- reading, testing and preliminary processing of entry data,
- placing the cells with tracing the connections and creating the data used in metalisations design program.

The "metalization design" part of system has 3 programs:
- reading, testing and preliminary processing of entry data,
- routing design in the all arrays channels,
- creating the data files for plotter and Pattern Generator.

Based on results of each program, user can trace the process of designing and overwrite some parameters in program if necessery. In particular, user has a possibility of placement appreciation between first and secound parts of system. The symbolic drawing of gate array allows to see the cells deposition.

The processing time is quadratic dependent on cells number, for placing algorithm. But for the program this dependence seems to be weaker. The program results are as follows:

No	1	2	3
number of cells	4	21	120
number of nets	12	26	84
CPU time in mins for placing	1.1	3.2	20.6
CPU time in mins for routing	7,6	28.4	81.6

Actual version of "MATRIX" system could design Gate Array up to 625 cells /25×25/ with 64 bonding pads. The sample layout drawing is presented /see Fig. 1/.