ON AUTOMATION PLACEMENT AND ROUTING OF GATE ARRAY

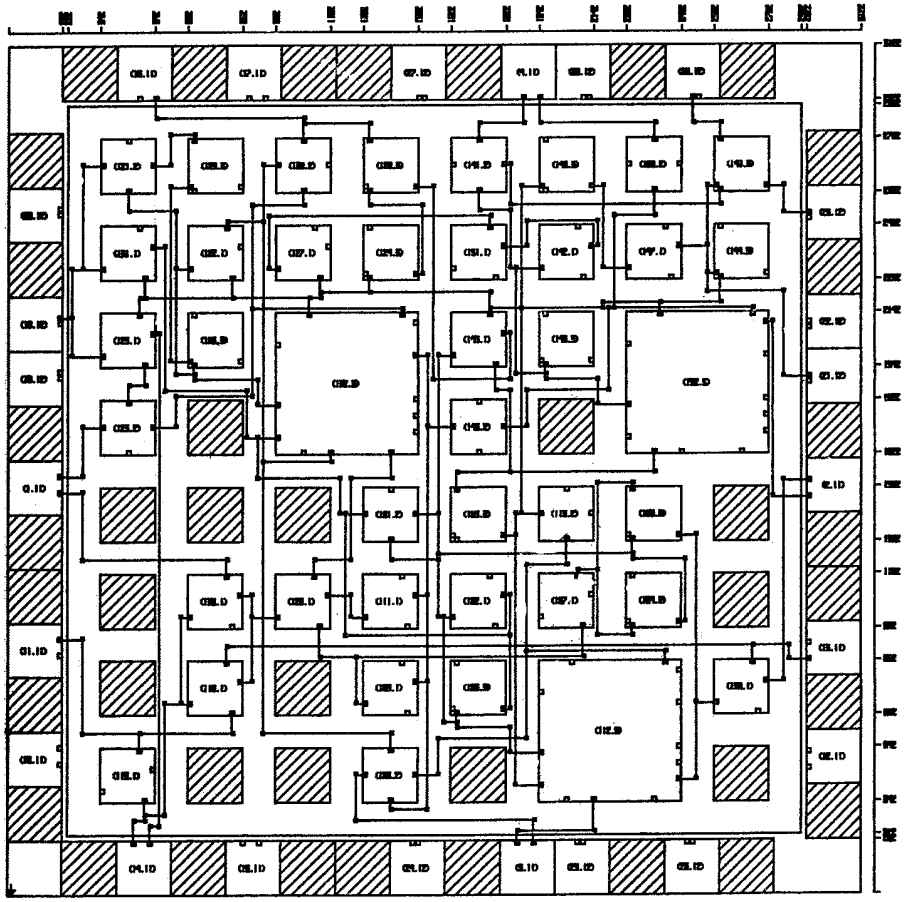
A.Wyszyński, R.Kubiak
Institute of Electron Technology, 02-668 Warszawa
Al.Lotników 38/46 POLAND

A method of fully automatic placement and routing of Gate Array is presented. The constructive placement is combined with tracing the connections. Next, the channel router generates the final routing, optimizing the number of layer changes and crossings. The results of the presented method's implementation are included.

1. INTRODUCTION

The paper presents a CAD method of bipolar Gate Array design. The array consist of regulary placed, quasi-aquare cells with horizontal and vertical channels for leading the connections between them /see Fig. 1/.

Two layers for connections are permitted. The layout design has two steps :
- Simultaneous placement and initial tracing of connections.
- Final routing, defining the geometry of connections and partitioning of two metalization layers.



(0,0) MATR21 LAY 09-JAN-85 SCALE 2 PAGE 1

Fig.1 The test Gate Array layout drawing from a plotter. The Gate Array contains 64 cells and 52 bounding pads. Regulary placed cells arrange vertical and horizontal channels for leading connections. Supply and ground tracks are not plotted.

The placement is based on building up the array "cell by cell". Subsequently, the sets of unplaced cells and available places in the array are searched. Unoccupied cells laid in the neighbourhoods of the cells, which have already been placed, make the set of available places. Search is made for cells which have the greatest number of contacts not yet connected. A cell and a place are chosen on the basis of the minimum va-

The algorithm belongs to the group of constructive algorithms, the final result is obtained by adding successive cells to the group of cells already placed.

Target-function is the criterion of choosing a cell for placing. This function is based on the connection length between a cell to be placed and the one already loca-

$$N(k) \leq 8\,(n-k)$$

The total number of operations is the sum:

$$N_t = \sum_{k=1}^{n} N(k) \leq 8 \sum_{k=1}^{n} (n-k) =$$

$$= 8\left(\sum_{k=1}^{n} n - \sum_{k=1}^{n} k\right) = 8\left(n^2 - \frac{n(n+1)}{2}\right)$$

finally:

$N \sim n^2$

- The obtained paths of connections must not effect on decrease production gain. This depends fully on the first two demands and minimum number of paths turnings.

3.2. The simplifications of the problem.

It is very difficult to obtain solution with the best electrical parameters of I.C. and with the highest production gain. The main problems to overcome are: defining precise algorithm's target function /many significant factors/ and time computing limitation. However in reality a "feasible" rather then an optimum solution is searched. It is pos-

a)

the target-function by taking into account the most powerful parameters only. So simp-

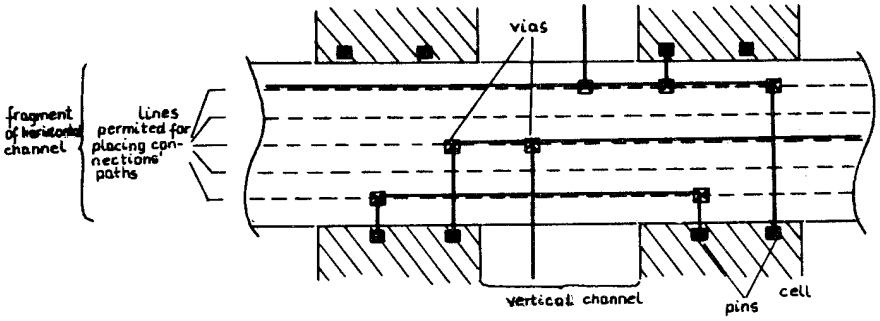


Fig. 5 Enlargement of channel's fragment. By dots are designed axises of connestions' paths.

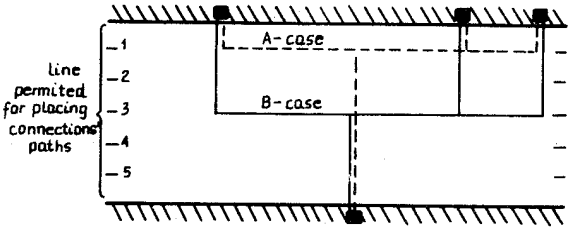


Fig. 6 Connection's path length is determinated by distance between chosen line and connection's pins. In A-case /chosen line no. 1/ the total length is lower than in B-case /chosen line no. 3/.

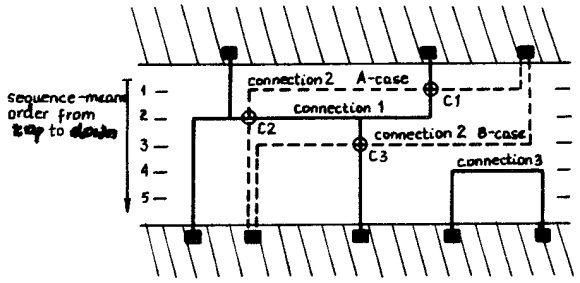


Fig. 7 Number of path crossing is determinated by sequence of chosen line in relation to other paths'lines. For connection no. 1 there are two orders /from top to down / :
A-case, sequence 2-1, crossings C1 and C2,
B-case, sequence 1-2, crossing C3.

This sequence is established at first for the given channel. In the next step, rectilinear segments of paths are placed on lines of channels preserving the previous sequence. If the segment of path could be located on one of several lines, this line is chosen, which assures the lowest path length.

4. FINAL RESULTS

The system based on the principles of the presented method is called "MATRIX". It has been programmed in FORTRAN IV and implemented on ODRA 1305 /ICL 1900/ computer under GEORGE-3 control. The system is fully automatic. The user can interact between programs only. If not satisfied he can overwrite some parameters for next step. There is no graphical interaction.

The final results of the system are as follows:
- the array's drawing with an exact design of metalization paths,
- the data file describing the metal mask of array. This file is used for Pattern Generator control.

The system consists of 5 programs and occupied the memory of maximum 48 K 24 bits words,

The "placement" part of system consists of 2 programs:
- reading, testing and preliminary processing of entry data,
- placing the cells with tracing the connections and creating the data used in metalisations design program.

The "metalization design" part of system has 3 programs:
- reading, testing and preliminary processing of entry data,
- routing design in the all arrays channels,
- creating the data files for plotter and Pattern Generator.

Based on results of each program, user can trace the process of designing and overwrite some parameters in program if necessery. In particular, user has a possibility of placement appreciation between first and secound parts of system. The symbolic drawing of gate array allows to see the cells deposition.

The processing time is quadratic dependent on cells number, for placing algorithm. But for the program this dependence seems to be weaker. The program results are as follows:

No	1	2	3
number of cells	4	21	120
number of nets	12	26	84
CPU time in mins for placing	1.1	3.2	20.6
CPU time in mins for routing	7,6	28.4	81.6

Actual version of "MATRIX" system could design Gate Array up to 625 cells /25×25/ with 64 bonding pads. The sample layout drawing is presented /see Fig. 1/.