occur between the 10th and 11th FP orders of FFP_2 indicating a properly designed second filter. A portion of the apparent 4dB loss at the adjacent FP orders of FFP_1 and most of the 15dB loss of FFP_2 is due to the 0·1nm resolution (13GHz) of the optical spectrum analyser. In the cascaded response shown in Fig. 2*b*, all FP orders of both filters are completely eliminated. Excellent locking characteristics were obtained with no isolator between the filters, and with both controllers operating with a nominal dither frequency of 2–4kHz. Power was measured at (B) and (C) in Fig. 1 with −16·7dBm power input at (A). Total insertion loss of the cascaded filter was measured at 5·6dB with FFP_2 preceeding FFP_1 and verified by spectra shown in Fig. 3*a*. Known losses in the cascaded filter were 3·2dB for the FFPs and 1·0dB for the two splitters (10% each) leaving 1·4dB for three connectors and the excess loss for two splitters. Wavelength locking was achieved with as much as 26dB attenuation of the input signal at (A) also shown in Fig. 3*a*. When FFP_1 preceeded FFP_2, the total measured insertion loss of the cascade was anomalously high at 8·6dB. Apparently, dithering of the wider band filter caused an additional average loss in the narrower band filter. Wavelength-locking of the cascaded filter was verified by changing the temperature of the DFB laser source thereby generating the curves of Fig. 3*b*.

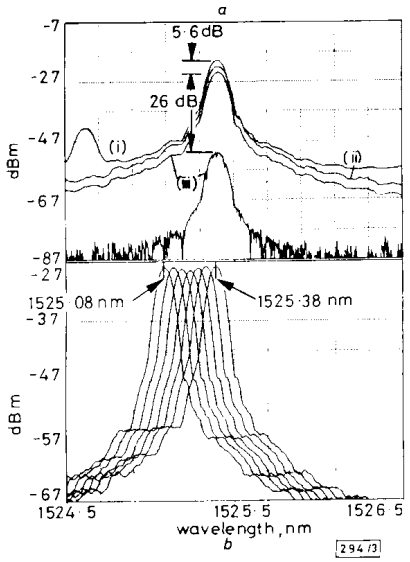

Fig. 3 *2nm output spectrum of cascaded FFP filter showing insertion loss of 5·6dB and dynamic range of 26dB, and wavelength locking with 0·3nm source drift*

a 5·6dB insertion loss and 26dB dynamic range
(i) laser
(ii) laser + FFP_2
(iii) laser + FFP_2 with 26dB added attenuation
b Wavelength locking with 0·3nm source drift

Summary: A two-stage FFP filter consisting of all commercially available components has demonstrated characteristics necessary to separate 1000 channels in an EDFA spectrum.

C. M. Miller and J. W. Miller (*Micron Optics, Inc., 2801 Buford Highway, Suite 140, Atlanta, GA 30329, USA*)

References

1 MIKKELSEN, B., *et al.*: 'High receiver sensitivity at 2·5Gb/s obtained with a highly efficient low noise diode pumped erbium doped fiber amplifier'. Proc. 2nd Conf. on Optical Amplifiers, paper FA4, Snowmass Village, July 1991, pp. 192–195

2 GABLA, P. M., LECLERC, E., and COEURJOLLY, C.: 'Practical implementation of a highly sensitive receiver using an erbium doped fiber preamplifier', *Photonics Technol. Lett.*, August 1991, **3**, (8), pp. 727–729

3 PARK, Y. K., GRANLUND, S. W., and DELAVAUX, J.-M. P.: 'Long distance transmission with erbium-doped fiber amplifiers in direct and coherent detection system'. Proc. (Invited Papers) 17th European Conf. of Optical Communication, Paris, September 1991, pp. 87–94

4 MILLER, C. M., and JANNIELLO, F. J.: 'Passively temperature compensated fibre Fabry–Perot filter and its application in wavelength division multiple access computer network', *Electron. Lett.*, 1990, **26**, (25), pp. 2122–2123

5 HUMBLET, P., and HAMDY, W.: 'Crosstalk analysis and filter optimization of single and double-cavity Fabry–Perot filters', *IEEE J. Sel. Areas Commun.*, 1990, **SAC-8**, (6), pp. 1095–1107

6 MILLER, C. M.: 'Low-loss cascaded fiber Fabry–Perot filter with finesse greater than 3,500'. Proc. (Part 1) 17th European Conf. on Optical Communication, Paris, September 1991, pp. 141–144

USING MULTIPLE-INPUT TRANSCONDUCTORS TO REDUCE NUMBER OF COMPONENTS IN OTA-C FILTER DESIGN

A. Wyszynski and R. Schaumann

Indexing terms: Transconductors, Integrated circuits, Filters, Operational amplifiers

Depending on the structure of the OTA and the topology of an OTA-C filter, the use of multiple-input OTAs can reduce the number of components, silicon area, and power dissipation by approximately a factor k, where k is the number of inputs of the OTA. A suitable bipolar OTA is presented, together with an example of ladder synthesis.

Introduction: The number of components in integrated analogue interface systems for VLSI signal processing is constantly growing. Although the analogue circuitry is usually confined to a small part on the digital chip, the number of components and the total power dissipated in the analogue part has long ceased to be negligible. This is true especially in high-frequency circuits which are built with operational transconductance amplifiers and capacitors, OTA-C circuits. In these designs, the majority of components is used to build highly linear, tunable and frequency compensated gain blocks, OTAs. With increasing OTA requirements, the number of components unavoidably grows. There are many examples of such cells in the literature [1–3, *]. None of them addresses the need of saving components and power.

Generally, fully-balanced designs prove to be superior to single-ended ones because of reduced offset, distortion, noise, nonlinearities and improved power supply rejection [2, 7, *]. However, the price for using a differential structure is roughly double the number of circuit components. Moreover, because the output DC level in a fully-balanced circuit is not defined, an additional common-mode feedback (CMF) circuit has to be added [4, 5]. This further increases the number of components, because a good CMF circuit, such as the one in Fig. 3, may be comparable in size with the OTA. Finally, the larger number of components results in increased vulnerability to layout parasitics, crosstalk or distortion caused by the extended connection lengths, nonuniformity of temperature, doping, and electrical conditions across remote parts of the system on the chip. Bearing these arguments in mind, reducing the number of elements in contemporary analog circuits seems to be a task of prime importance.

Method of saving components: OTAs with multiple inputs have been used for various reasons, such as facilitating signal addition, improving the output impedance, and obtaining superior noise performance [7, 8], but the possibility of reducing circuit complexity seems not to have been recognised or systematically exploited.

The idea of saving components in OTA-C filter synthesis is as follows: given an arrangement of OTAs and capacitors

* SZCZEPANSKI, S., WYSZYNSKI, A., and SCHAUMANN, R.: 'Highly linear voltage-controlled CMOS transconductors', submitted to *IEEE Trans. Circuit and Systems*, 1991

which realise an OTA-C filter by ladder simulation or cascading of biquad sections, frequently two or more OTAs have their outputs connected together to a current summing node. This configuration, presented in Fig. 1 for two OTAs, is equivalent to a single OTA with two inputs and one common output.

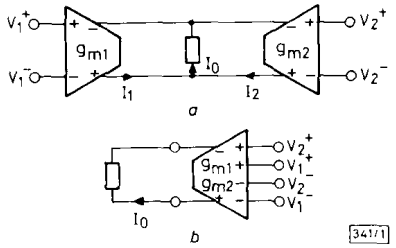

Fig. 1 *Circuit diagram for two single-input OTAs and one double-input OTA*

a Two single-input OTAs
b One double-input OTA

Adding the output currents of the two OTAs in Fig. 1*a* yields

$$I_0 = I_1 + I_2 = g_{m1}(V_1^+ - V_1^-) + g_{m2}(V_2^+ - V_2^-) \qquad (1)$$

which is the equation for the double-input OTA cell in Fig. 1*b*. Assuming that $g_{m1} = g_{m2} = g_m$ as happens in most OTA-C designs, eqn. 1 takes the form

$$I_0 = g_m[(V_1^+ + V_2^+) - (V_1^- + V_2^-)] \qquad (2)$$

Eqn. 2 can also be interpreted in a slightly different way: assuming appropriate voltage summing circuitry is available, the sum of different voltages can be applied to one single-input OTA, resulting in substantial component savings.

If k identical OTAs have a common output, and are combined to a multiple-input OTA with k inputs, the number of components required is $N_k = N_1 + l(k-1)$, where N_1 is the number of elements in a single-input OTA, and l is the number of components used by each of the additional multiple inputs. Reasoning this way, a total saving of components, S = (number of components)/(reduced number of components), can be calculated as

$$S = \frac{kN_1}{N_1 + (k-1)l} \simeq k \qquad (3)$$

Eqn. 3 assumes that $(k-1)l \ll N_1$, i.e. it follows that a suitable circuitry for an OTA should add the smallest possible number of elements per each additional input. In this case, component savings by, in the limit, a factor k take place. When the condition is not fulfilled, savings also occur but they are more modest.

Filter synthesis with multiple-input OTAs: As a simple illustration of using the above technique, consider the synthesis of a third-order elliptic filter. Its ladder and single-input fully-balanced models are presented in Fig. 2*a* and *b*. By grouping OTA2 with OTA3, OTA4 with OTA5, and OTA6 with OTA7 as having common outputs, three double-input OTAs: OTA23, OTA45, and OTA67 are identified and connected as in Fig. 2*c*.

Because of the voltage divider $R_L/(R_S + R_L)$ the RLC model in Fig. 2*a* has a -6 dB flat loss. To compensate for this loss, the g_m value of OTA1 in the single-input realisation of the filter should be doubled, which is conveniently realised by connecting two OTAs in parallel. This is equivalent to the double-ended OTA11 in Fig. 2*c*, with its inputs tied together.

The total count after the conversion is four double-input OTAs instead of eight single-input OTAs. Clearly, if the double-input OTA consisted of approximately the same

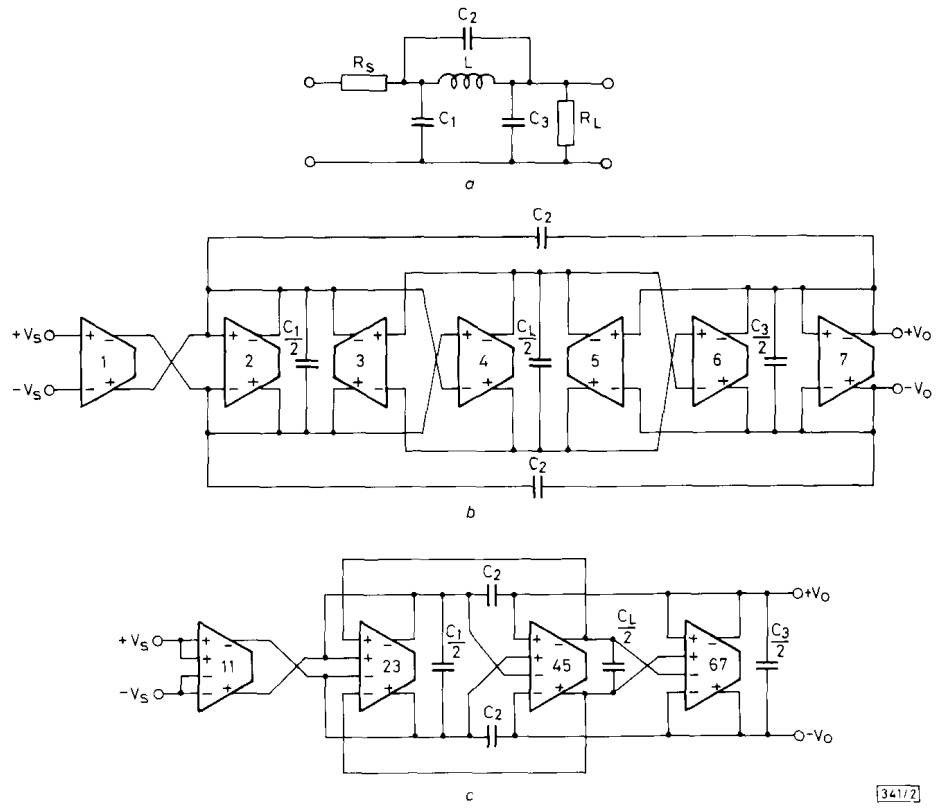

Fig. 2 *Circuit diagram for third-order elliptic low pass filter*

a Passive prototype ladder
b With single-input OTAs and capacitors
c With double-input OTAs and capacitors

number of components as the single-input OTA, savings by nearly one half in the number of components would result.

It is possible to extend this procedure to practically all OTA-C structures; in some of them OTAs with more than two differential inputs can be used. For example it is noted that OTA11 and OTA23 in Fig. 2*c* share a common output. Thus, a four-input OTA could be substituted for additional savings of components, but the OTAs would no longer be identical. The general problems and procedures of OTA-C filter synthesis using multiple-input OTAs are being currently investigated.

Multiple-input OTA cell: The circuit in Fig. 3 represents a suitable solution for a multiple-input OTA according to the previously established guidelines: it uses only two additional transistors and two resistors for the second input pair. Its single-input operation has been described elsewhere† and will not be repeated. It should be pointed out here that the OTA is fully-tunable, and its differential transconductance is given by

$$g_m = \frac{1}{2R_1}\frac{I_{E2}}{I_{E1}} \tag{4}$$

Using an 8 GHz bipolar transistor array process, the OTA has a -3 dB frequency of more than 2·7 GHz, and a maximum linear input range of $\pm 2{\cdot}5$ V for a power supply of ± 5 V. The circuit consists of total of 22 transistors and 16 resistors, of which eight transistors and eight resistors form the CMF circuit. For the double-input structure, linearity, input and output impedance, power consumption and bandwidth stay almost the same as for the single-input configuration.

An additional advantage of using multiple-input transconductors in OTA-C filter design is a reduction of parasitic capacitances associated with the OTA. It can be shown that for the filter in Fig. 2*c* parasitics associated with the capacitors C_1, C_L and C_3 are less than for the filter in Fig. 2*b*. It is due to parasitics of the output stage in a double-input OTA being theoretically half of those of two single-input OTAs. This in turn allows designs with smaller values of capacitors and may permits a higher cut-off frequency of the filter, given the maximum value of g_m [9].

Conclusion: The idea of saving components, and reducing power consumption and circuit parasitics by using miltiple-input OTAs in OTA-C filter design has been presented. Theoretically it can lead to reducing the area occupied by a filter and the power consumption by a factor k, where k is the number of inputs per OTA. The values of savings obtainable in practice strongly depend on the structure of the filter and the OTA cell. It can be also shown that this method leads to a reduction of layout parasitics due to shorter connections on a smaller occupied area, and circuit parasitics. This makes the technique preferable for VHF filter design.

In an application of this method for an OTA-C filter design, double-input OTAs were used. The numbers of components, chip area and the total power consumption were nearly halved. A practical benefit of applying double-input OTAs, on a transistor-array chip of a given size, was the realisation of a fifth-order elliptic filter with cutoff frequency of 250 MHz and attenuation better than 50 dB. Originally, using single-output OTAs, the chip could barely accommodate a third-order elliptic filter, with the same cutoff frequency, but with attenuation of only 22 dB.

Acknowledgment: This work was supported in part by a 1991/92 Tektronix Fellowship.

18th November 1991

A. Wyszynski and R. Schaumann (*Department of Electrical and Computer Engineering, Portland State University, PO Box 751, Portland, Oregon, 97207-0751, USA*)

† WYSZYNSKI, A., SCHAUMANN, R., SZCZEPANSKI, S., and VAN HALEN, P.: 'Design of a 2·7 GHz linear OTA and a 250 MHz elliptic filter in bipolar transistor-array technology with lateral PNPs submitted to *IEEE Trans. Circuit and Systems*, 1991

References

1 PARK, C.-S., and SCHAUMANN, R.: 'Design of a 4 MHz analog integrated CMOS transconductance-C bandpass filter', *IEEE J. Solid-State Circuits*, 1988, **SC-23**, pp. 987–996

2 KRUMMENACHER, F., and JOEHL, N.: 'A 4-MHz CMOS continuous-time filter with on-chip automatic tuning', *IEEE J. Solid-State Circuits*, 1988, **SC-33**, pp. 750–758

3 DEVEIRMAN, G. A., and YAMASAKI, R.: 'Fully-integrated 5 to 15 MHz programmable Bessel lowpass filter'. Proc. IEEE Int. Symp. Circ. Syst., 1990, pp. 1155–1158

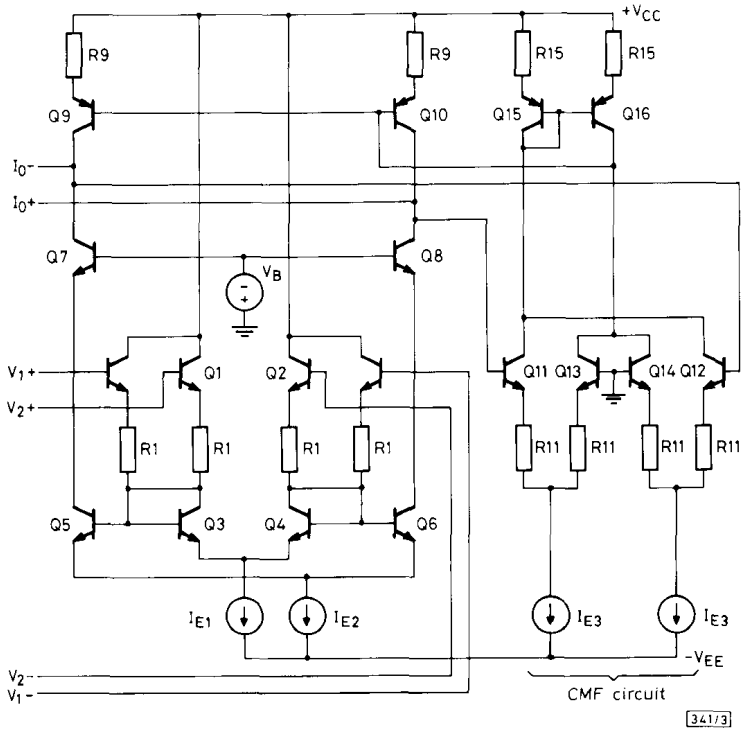

Fig. 3 *Diagram for double-input OTA with CMF circuit*

4 VAN PETEGHEM, P., and DUQUE-CARRILLO, J.: 'A general description of common-mode feedback in fully integrated amplifiers'. Proc. IEEE Int. Symp. Circ. Syst., 1990, pp. 3209–3212
5 WU, P., SCHAUMANN, R., and LATHAM, P.: 'Design considerations for common-mode feedback circuits in fully-differential operation transconductance amplifiers with tuning'. Proc. IEEE Int. Symp. Circ. Syst., 1991, pp. 1363–1366
6 BANU, M., and TSIVIDIS, T.: 'Fully integrated active RC filters in MOS technology', *IEEE J. Solid-State Circuits*, 1983, **SC-18**, pp. 644–651
7 GOPINATHAN, V., TSIVIDIS, Y. P., TAN, K.-S., and HESTER, R. K.: 'Design considerations for high-frequency continuous-time filters and implementation of an antialiasing filter for digital video', *IEEE J. Solid-State Circuits*, 1990, **SC-25**, pp. 1368–1378
8 DEVEIRMAN, G. A., and YAMASAKI, R.: 'Monolithic 10–30 MHz bipolar Bessel lowpass filter'. Proc. IEEE Int. Symp. Circ. Syst., 1991, pp. 1444–1447
9 WU, P., and SCHAUMANN, R.: 'A 200 MHz elliptic OTA-C filter in GaAs technology'. Proc. IEEE Int. Symp. Circ. Syst., 1991, pp. 1745–1748

IMPROVED RECOGNITION CAPABILITIES FOR GOAL SEEKING NEURON

R. G. Bowmaker and G. G. Coghill

Indexing term: Neural networks

RAM based neural networks are a relatively new class of neural network which exhibit faster learning and greater ease of VLSI implementation than the traditional analogue models. Two RAM based neural models, the probabilistic logic neuron (PLN) and the goal seeking neuron (GSN), are simulated to determine their recognition capabilities. It is found that the PLN has very poor capabilities, whereas the GSN has widely varying capabilities due to the random nature of the GSN learning algorithm. A new GSN learning algorithm is presented which gives consistently good results.

Introduction: The vast majority of artificial neural network research and application deals with the traditional analogue neural model. Analogue networks have a number of advantageous characteristics, including intrinsic generalisation abilities. The disadvantages of analogue neural models typically include slow training and difficulty of VLSI implementation. RAM based neural networks are a relatively new class of neural network which overcome these disadvantages [1]. This Letter answers the question of whether RAM based neural networks can be made to exhibit, in some sense, the important generalisation ability of analogue networks.

The first popular RAM based neural model was the probabilistic logic neuron (PLN) proposed by Kan and Aleksander [2]. The PLN is a very simple model, and is therefore very easy to implement. GSN networks suffer, however, from the problems of nondeterministic response, saturation of learning space, and poor generalisation ability [3].

The goal seeking neuron (GSN) is a more complex RAM based neural model proposed by Filho *et al.* to overcome the limitations of the PLN [4, 5]. A GSN network has a deterministic response, makes more efficient use of the limited storage space of a RAM-based neuron, and has some intrinsic generalisation abilities.

Nonrandom learning: The operation of the GSN is deterministic, except for the learning state of the neuron. When there is more than one possible location to write the desired output value to, a random decision is made. This means that two identical GSN networks, trained with the same data, could have different recognition properties due to different decisions being made during the learn phase of the network.

It was found that to implement such a random decision would be difficult using digital logic, and would make the performance of the GSN network inconsistent in the manner mentioned above. For these reasons, the following alternative methods of choosing a location were evaluated as alternatives to the random method:

(1) choose the first applicable cell when arranged in numerical order of cell addresses

(2) If the desired output of the pyramid is 0, choose the applicable cell whose address is closest to 00 ... 0 (i.e. all 0s) in terms of Hamming distance; if the desired output of the pyramid is 1, choose the applicable cell whose address is closest to 11 ... 1 (i.e. all 1s) in terms of Hamming distance.

The first method was evaluated for its simplicity and ease of implementation. The second was designed to force the network to make the internal representations of patterns which are to be associated with the same output value as similar as possible to each other and the internal representations of patterns which are to be associated with different output values as different as possible to each other. This should have the effect of improving the ability of the network to differentiate between separate classes, and generalise between members of the same class.

Network simulations: Computer simulations of PLN and GSN networks were carried out using the two nonrandom learning approaches presented above to test the generalisation ability of the different networks. Each network consisted of eight pyramids of four levels each, with a neuron connectivity of 4. The resulting input space of the networks was 256 bits, arranged as a 16 × 16 grid of binary values. The training data consisted of eight, 16 × 16 character patterns, each with a Hamming distance of 48 bits from all of the other patterns. The networks were trained such that each of the eight pyramids was to respond with a 1 for its respective character, and 0 for all the other characters.

The recognition capability of each of the networks was tested by corrupting (i.e. logically inverting) n bits of the first character pattern in random positions, where n ranged from 0 to 49. For each value of n, 1000 randomly corrupted patterns were sequentially applied to the input of the network. Because the input pattern was a corrupted version of the first pattern, only the first pyramid should have responded with a 1. All other network outputs were considered to be erroneous. The number of erroneous outputs per 1000 input patterns was recorded as the error rate for the particular level of corruption.

This test was designed solely as a means of comparing the different neural networks. The types of corruption encountered in real applications, such as blurring, interference or aliasing, may have significantly different characteristics to the random corruption used in this test.

Fig. 1 shows the results of the simulations as a graph of the recognition error rate as a percentage (out of 1000) against the level of corruption as a percentage (of 256 bits).

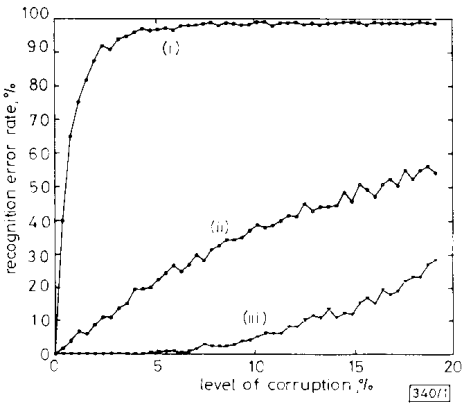

Fig. 1 *Results of recognition capability test*
(i) probabilistic logical neuron
(ii) goal seeking neuron (1)
(iii) goal seeking neuron (2)