In Fig. 2, signals obtained when a mild steel block containing a circular-arc saw-cut notch (simulating a crack) with d_0 = 5mm and p = 18mm was scanned, are shown. In this case, the sensor was attached to an inducer with two U-shaped wires (Fig. 1). The signal in Fig. 2*a*, which is for a scan normal to the notch lips along the centre line, clearly shows a discontinuity. The discontinuity occurs when the sensor is at the crack lips. It was found that the magnitude of this discontinuity depends on the crack depth. The signal in Fig. 2*b* which is for a scan parallel to the lips shows two peaks corresponding to the two ends of the crack. This signal can be used to find the crack length p. The theoretical signals for the above cases are also obtained and displayed in the same Figures. Good agreement between the theory and measurement is evident.

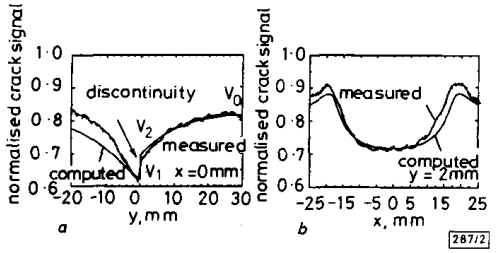

Fig. 2 *Theoretical and experimental crack signals when the circular-arc saw-cut notch was scanned*

a Normal
b Parallel to its lips by the indicer-sensor arrangement shown in Fig. 1*a*
a = 10mm, b = 4mm, l = 80mm, h = 20mm, D_s = 13mm, p = 18mm and d_0 = 5mm

Crack measurement: One of the superb features of the SMFM technique is its unique capability in sizing cracks without resorting to calibration and calibration standards. This feature stems from the presence of a thin skin eddy current in the metal which makes the effect of the variation of skin depth near a crack of second order in the magnetic field distribution above the work piece. In other words, the conductivity of the metal does not play a role in this technique and therefore the technique does not require any calibration. This feature is important for two reasons, first, there are many occasions when the conductivity of metal under test is not available nor can it be easily evaluated, and secondly, the current distribution around a crack can be basically considered two dimensional and hence its theoretical modelling is easier than modelling a three-dimensional eddy current.

When dealing with steel structures, the permeability μ_r is large and as long as condition $l << \mu_r\delta$ (where δ is the skin depth and l is the smallest crack dimension) is satisfied, it can be shown that the magnetic field has a Laplacian distribution both at the metal surface and at the two faces of the crack [2]. In other words, the magnetic field at the metal surface can be derived from equations $\mathbf{H}$ = grad ϕ where ϕ is the solution of $\Delta\phi = 0$ subject to boundary conditions. The solution of this problem for circular-arc cracks has been given by the authors and can be found in [3]. Based on the solution, a computer program has been developed which can compute the current and the magnetic field distributions around a crack. This program has been used to produce inversion curves. For different inducers and sensor locations, the inversion curves are different.

Typical inversion curves are shown in Fig. 3 for a specific inducer when the scan is along the crack centre line normal to crack lips. R_s on the ordinate is the percentage of signal change given by $R_s = (V_2 - V_1)/V_1$ where V_2 and V_1 are shown in Fig. 2*a*. To find the depth of a crack using the curves in Fig. 3, first the crack length is measured using a parallel scan, Fig. 1, and then a normal scan is made along the crack centre line to find R_s.

For welded regions where a normal scan is difficult, a different approach can be adopted to find the crack depth. Two scans are made parallel to the weld, one close to the weld and one far from it. From the signal of the close scan, the crack length and V_2 can be obtained and from that of the remote scan V_0, V_2 and V_0 are shown in Fig. 2*a*. This information can then be used to evaluate the crack depth using a set of inversion curves based on $r = (V_2 - V_0)/V_0$ and crack length p. Owing to a lack of space, these curves are not given here.

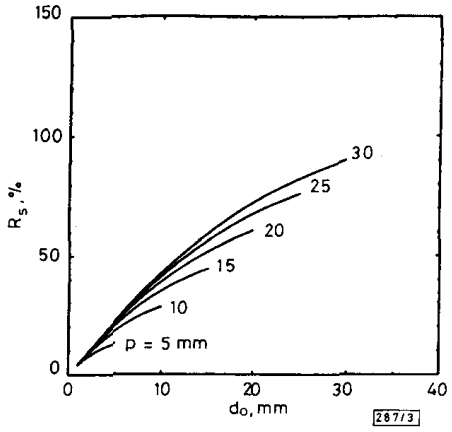

Fig. 3 *Inversion curves for a sensor-inducer arrangement in which the inducer consists of two U-shaped wires and the sensor is attached to the inducer as shown in Fig. 1*

h = 10mm, l = 70mm, a = 8mm, b = 5mm, D_s = 10.5mm

Conclusions: The principles of a new electromagnetic technique for detecting and measuring surface breaking cracks in metal structures were outlined and some example results were presented. Also, two methods for inverting crack signals to crack dimensions, were addressed. The important features of the technique are the simplicity of instrumentation, ease of use and independence from various calibrations.

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References

1 SADEGHI, S.H.H., and MIRSHEKAR-SYAHKAL, D.: 'A new technique for sizing cracks in metals, utilising an induced surface magnetic field', *in* 'Review of progress in quantitative nondestructive evaluation, Vol. 9' THOMPSON, D.O., and CHIMENTI, D.E. (Eds.) (New York: Plenum Press), 1990, pp. 593–600

2 LEWIS, A.M., MICHAEL, D.H., LUGG, M.C., and COLLINS, R.: 'Thin skin electromagnetic fields around surface-breaking cracks in metals', *J. Appl. Phys.*, 1988, , pp. 3777–3784

3 SADEGHI, S.H.H., and MIRSHEKAR-SYAHKAL, D.: 'Scattering of an induced surface electromagnetic field by fatigue cracks in ferromagnetic metals', *IEEE Trans.*, 1992, **MAG-28**, pp. 1008–1016

Low-voltage CMOS and BiCMOS triode transconductors and integrators with gain-enhanced linearity and output impedance

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Indexing terms: Integrated circuits, Transconductors

CMOS and BiCMOS mode transconductors and integrators achieving a simulated THD of 0.03% for differential input signals of 0.5V peak to peak with a supply voltage of 2.5V are presented. Small phase errors and high g_m tunable by a factor of 10 allow the circuits to be used in continuous-time filters working at 100MHz.

Introduction: With the scaling down of supply voltages, low-voltage linear transconductors (G_Ms) and integrators are required. A

constant g_m (undefined symbols in this Letter have their usual meaning) of a triode MOS device with constant V_{DS} allows us to build mode linear transconductors [1–5]. In the following, a substantial linearity improvement in a mode transconductor is presented which makes use of an additional gain stage to increase the g_m of the cascode device controlling the V_{DS} of the triode MOS device. Active feedback was also applied in [1] and [2] to stabilise the V_{DS} of the mode transistor, but the implementation presented here, based on a regulated cascode, results in higher gain, and therefore in better linearity. A regulated cascode was used in [6] to enhance the gain of voltage amplifiers and in [7] to obtain a high-swing and high-output-impedance current source, but the implementation of linear triode transconductors seems not to have been recognised or systematically exploited. The advantages of the presented approach enable us to realise an all-CMOS transconductor with high linearity, high output impedance and a supply voltage of only 2.5V. BiCMOS transconductors based on this principle have even better linearity and bandwidth.

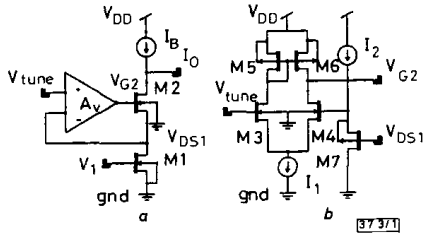

Fig. 1 *Low-voltage linearity-enhanced triode transconductor*

a CMOS transconductor (G_M)
b CMOS gain-stage (OTA)

CMOS and BiCMOS transconductors: Consider the CMOS transconductor in Fig. 1*a*. Using a simplified expression for I_{D1} in the triode region, $I_{D1} \simeq k_1(V_{GS1} - V_{th} - V_{DS}/2)V_{DS}$, with $k_1 = \mu C_{ox} (W/L)_1$, the transconductance can be shown to be approximated by

$$g_m \simeq \frac{k_1 V_{DS1}}{1 + \frac{V_{GS2} - V_{th}}{A_v V_{DS1}}} = \frac{g_{m1}}{1 + \frac{2I_{D1}}{A_v g_{m2} V_{DS1}}} \qquad (1)$$

From eqn. 1 and Fig. 1*a*, $g_m \simeq k_1 V_{DS1}$ is linear and can be tuned by V_{tune}. The presence of A_v increases the effective transconductance of M_2 A_v times and reduces the linearity error $\varepsilon \simeq (2I_{D1})/(A_v g_{m2} V_{DS1})$. Additional linearity errors exist due to the assumption that $(V_{GS1} - V_{th}) >> V_{DS1}/2$ and because of mobility saturation given by $\mu \simeq \mu_o/[1 + \Theta (V_{GS} - V_{th})]$. These errors can be reduced in fully-diiferential structures, such as that shown in Fig. 2*a* for a BiCMOS implementation. If M_2 in Fig. 1*a* is replaced by a bipolar device Q_2, the linearity error $\varepsilon \simeq I_{D1}/(A_v g_{m2} V_{DS1})$ is smaller because bipolar g_{m2} is larger compared to that of M_2.

Multiple-input transconductors are obtained simply by adding additional input mode MOS devices. As shown in Fig. 2*b*, a realisation of a tunable G_M loaded with a tunable $1/G_M$ resistor is obtained by connecting one input to the output. Being linear even as single-ended structures, triode transconductors are well suited for certain applications in continuous-time filters [8].

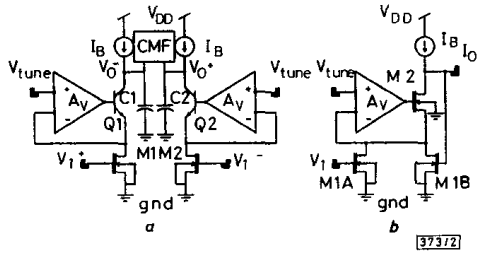

Fig. 2 *Practical implementations in CMOS and BiCMOS technology*

a BiCMOS differential integrator with a CMF circuit
b CMOS G_M loaded by $1/G_M$ tunable load resistor

Assuming an ideal current source I_B, the output resistance of G_M in Fig. 1*a* is given by $R_o \simeq (r_{o2} A_v g_{m2})/g_{m1}$. The increase of R_o by the factor A_v is achieved without an additional cascode stage that would increase the required supply voltage. R_o for BiCMOS design is approximated by the same formula, but the effective gain A_v of the BiCMOS amplifier is reduced due to the loading effect of Q_2. In practical circuits, I_B is realised by a *p*MOS cascode current source. I_B is set by a common-mode feedback (CMF) circuit as shown in Fig. 2*a*. A_v in Fig. 1*a* is realised as a simple differential OTA shown in Fig. 1*b*. It consists of a CMOS (BiCMOS) differential pair, $M_3 - M_4$ ($Q_3 - Q_4$), an active *p*MOS load $M_5 - M_6$, and a *p*MOS emitter-follower M_7 as a level shift at the inverting input.

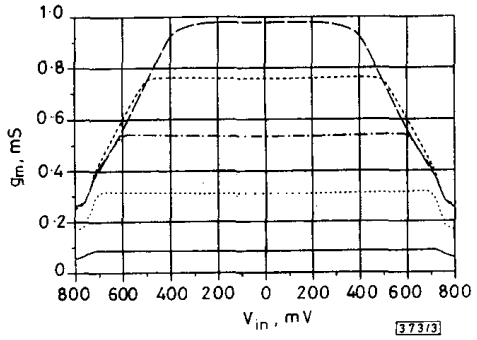

Fig. 3 *Linearity and tunability of differential G_M built with two CMOS stages in Fig. 1a*

V_{tune}
——— 875mV
····· 950mV
– · – · 1.03V
- - - - 1.10V
– – – – 1.18V

Simulation results: The presented transconductors have been extensively simulated on SPICE using Level 3 models with a minimal length of an MOS device of 1.2μm, k_n = 120.2μA/V², k_p =35.6μA/V², V_{in} = 0.789V, V_{tp} = –0.868V, and bipolar devices with f_T = 8GHz. For the CMOS OTA in Fig. 1*b*, the simulated gain $A_v \simeq$ 51dB and $f_{3dB} \simeq$ 6MHz give $GBW \simeq$ 2.1GHz, whereas the BiCMOS OTA, due to the higher g_m of a bipolar input pair, has $A_v \simeq$ 55dB, $f_{3dB} \simeq$ 18MHz and $GBW \simeq$ 10GHz.

The linearity and tunability of the differential version of CMOS G_M in Fig. 1*a* are shown in Fig. 3. The performance of the BiCMOS G_M is similar. When V_{tune} changes from 875 to 1175mV, V_{DS1} varies from 31 to 357mV and g_m changes by a factor of more than 10 from 85 to 980μS maintaining high linearity. The simulated power dissipation is then between 2.3 and 8.2mW, and the linear range varies from 1.5 to 0.5V peak to peak for a power supply of 2.5V. For V_{tune} = 1100mV and differential input signals of 0.5V peak to peak at 10MHz, the simulated $THD \simeq$ 0.03% for both the CMOS and the BiCMOS G_M. For a differential input of 0.8V peak to peak at 10MHz, $THD \simeq$ 0.23% for the CMOS G_M and 0.08% for the BiCMOS G_M. The simulated DC gain of the integrator structure in Fig. 2*a* is 72dB for CMOS and 61dB for BiCMOS design. The simulated phase errors remain small up to several tens of megahertz for the CMOS integrator and up to 100MHz for the BiCMOS integrator. Phase errors can be further reduced by a phase compensation scheme.

Conclusions: Highly-linear CMOS and BiCMOS mode transconductors and integrators have been presented. They use additional simple OTA gain stages to boost the g_m of the cascode device. The OTAs introduce small phase errors to the overall frequency response. The integrators have high DC gain of 60 – 70dB due to enhanced output impedance. The small phase errors of the presented integrators and the high value of g_m (up to several millisiemens) enable VHF continuous-time filters to be realised for frequencies up to 100MHz for CMOS and several hundred megahertz for BiCMOS designs. The presented integrators are tunable by a factor of more than 10. They can operate with a low supply voltage of 2.5V. Multiple-input transconductors and tunable resistors have readily been obtained. The measured results of a filter chip containing the presented transconductors and integrators will be reported in a future publication.

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References

1 PENNOCK, J.L.: 'CMOS triode transconductor for continuous-time active integrated filters', *Electron. Lett.*, 1985, **21**, pp. 817–818
2 GATTI, U., MALOBERTI, F., and TORELLI, G.: 'A novel CMOS linear transconductance cell for continuous-time filters'. Proc. IEEE Int. Symp. Circ. Syst., 1990, pp. 1173–1176
3 CASTELLO, R., MONTECCHI, F., ALINI, R., and BASCHIROTTO, A.: 'A very linear BiCMOS transconductor for high-frequency filtering applications'. Proc. IEEE Int. Symp. Circ. Syst., 1990, pp. 1364–1367
4 STEFANELLI, B., and KAISER, A.: 'CMOS triode transconductor with high dynamic range', *Electron. Lett.*, 1990, **26**, pp. 880–881
5 NAUTA, B., KLUMPERINK, E., and KRUISKAMP, W.: 'A CMOS triode transconductor'. Proc. IEEE Int. Symp. Circ. Syst., 1991, pp. 2232–2235
6 SACKINGER, E., and GUGGENBUHL, W.: 'A high-swing, high-impendance MOS cascode circuit', *IEEE J. Solid-State Circuits*, 1990, **SC-25**, pp. 289–298
7 BULT, K., and GEELEN, G.J.: 'A fast-settling CMOS op amp for CS circuits with 90-dB DC gain', *IEEE J. Solid-State Circuits*, 1990, **SC-22**, pp. 1366–1384
8 WYSZYNSKI, A., and SCHAUMANN, R.: 'Frequency and phase tuning of continuous-time integrated filters using common-mode signals'. Submitted to IEEE Int. Symp. Circ. Syst., October 1993

New observation of charge injection in MOS analogue switches

M.-J. Chen, Y.-B. Gu, T. Wu, P.-C. Hsu and T.-H. Liu

Indexing terms: Integrated circuits, Switched capacitor networks

Based on experimental analogue MOS switches, the Letter reports a new observation of the charge injection component due to channel charges in weak inversion. As identified by the mixed-mode circuit and device simulations, this new component can contribute comparably to the switch-induced error voltage on a switched capacitor.

Introduction: Charge injection in analogue MOS switches has recently been studied extensively [1–4]. Suppression of the charge injection-induced error voltage on a switched holding capacitor is very important for switched-capacitor circuits. In this Letter we report a new observation of the charge injection component due to channel charges in weak inversion, which has not previously been observed experimentally or predicted theoretically.

Experimental observations: The on-chip test circuitry consists of one *n*-channel MOSFET, a holding capacitor C_H, and a unity-gain operational amplifier, as shown in Fig. 1. This test circuitry has been fabricated by a 1.2 μm double-metal double-polysilicon CMOS process. The gate voltage waveform $V_G(t)$ is given a pulse width t_w ranging from 1 μs to 100 μs and a fall time t_f from 6ns to 5μs. Because the unity-gain operational amplifier is used as a buffer, the waveform $V_H(t)$ on the holding capacitor can be represented by the measured waveform at the output. We have found that the new role of the channel charges in weak inversion is reproducible for a variety of the design parameters and measurement conditions. The case $W = 25\mu m$, $L = 4\mu m$, and $C_H = 1.0PF$, at the measurement condition of $V_{in} = 2V$, $t_w = 10\mu s$, and $t_f = 0.6\mu s$, is presented here. The corresponding observed waveforms at the gate and the output are shown in Fig. 1. Also shown in Fig. 1 is the waveform of the drain current $I_D(t)$. According to [1], the turn off of an MOS switch consists of two distinct phases: $t_1 < t < t_2$ and $t_2 < t < t_1 + t_f$ as labelled in Fig. 1. Here t_2 represents the

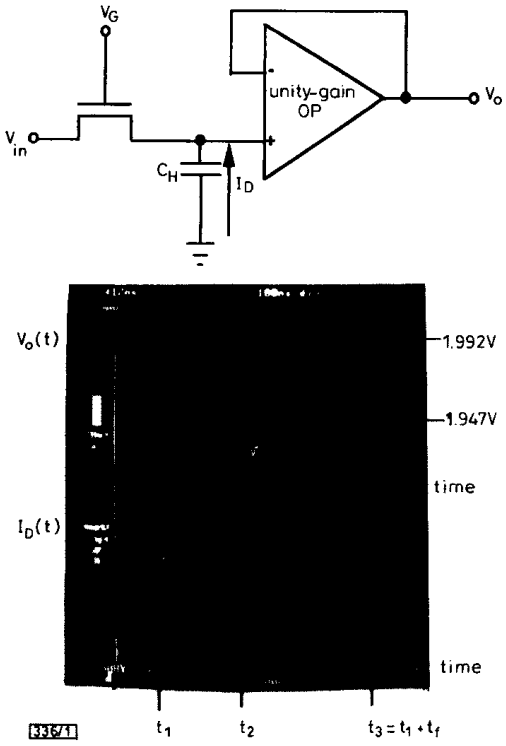

Fig. 1 *Schematic on-chip test circuity and measured voltage waveforms at gate and output*

Waveform $I_D(t)$ created by Tektronix 11402A is shown together. The horizontal scale is 100ns/division. The vertical scales for $V_G(t)$, $V_o(t)$, and ID(t) are 1V/division, 20mV/division, and 20nA/division, respectively. $t_1 = -300ns$, $t_2 = -40ns$, and $t_3 = 300ns$. The offset of the unity-gain opamp is ~8mv

time for the gate voltage $V_G(t)$ reaching the sum of the input voltage V_{in} and threshold voltage V_{th}. During the first phase, i.e. $t_1 < t < t_2$, some of the channel mobile charges are injected into the switched capacitor. At $t_1 = t_2$, the conduction channel disappears and the transistor enters the second phase of turn-off [1]. Therefore according to [1], the $I_D(t)$ curve for $t_2 < t < t_1 + t_f$ would be a constant because the $V_G(t)$ is a ramp voltage in this period. However, this is inconsistent with the $I_D(t)$ curve observed in Fig. 1 for $t_2 < t < t_1 + t_f$, where the drain current continuously decays with time until a constant one appears. Therefore during the second phase of the turn-off, in addition to the clock feedthrough through the gate-to-drain overlap capacitance [1], the channel charges in weak inversion should be taken into account.

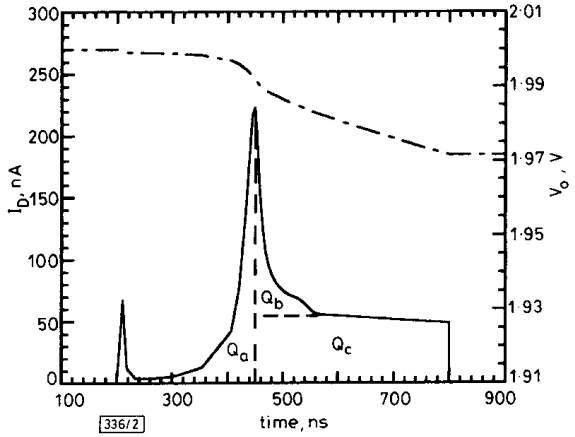

Fig. 2 *Simulated $V_o(t)$ and ID(t) waveforms under same conditions as Fig. 1*

$L = 4\mu m$, $W = 25\mu m$, $C_H = 1pF$, $t_f = 600ns$, $V_{in} = 2V$
——— I_D
– – – V_o