

VHF Highly Linear Fully-Balanced CMOS OTA

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Abstract - A fully-balanced, highly linear CMOS OTA based on a cross-coupled, voltage-tunable quad input circuit is presented. Simulations show that for a standard $2\ \mu$ CMOS technology with a power supply of $\pm 5V$, the linearity error is lower than 0.1% for an input voltage $\pm 2.5V$, the $-3\ \text{dB}$ frequency is over 1.5 GHz and the tuning range of g_m is $17\ \mu S$ to $202\ \mu S$. The simulated dynamic range of an integrator built with the above OTA is over 70 dB.

Many CMOS OTAs with good linearity [1] - [3] and wide bandwidth have been reported; among them, the cross-coupled input stage of the OTA in [3] combines superior linearity and very wide bandwidth but has a single-ended output. This presents a serious difficulty in any attempt to carry this linearity and bandwidth to the output. The deficiency is removed in the present work, making the resulting OTA a very convenient building block for VHF OTA-C filter design.

I. INTRODUCTION

In the design of very-high-frequency (VHF) analog filters, linear, wide-band, fully balanced operational transconductance amplifiers (OTAs) are required.

II. THE INPUT STAGE

The input-stage consists of two pMOS cross-coupled pairs $M1, M2$ and $M3, M4$ as shown in Fig. 1.

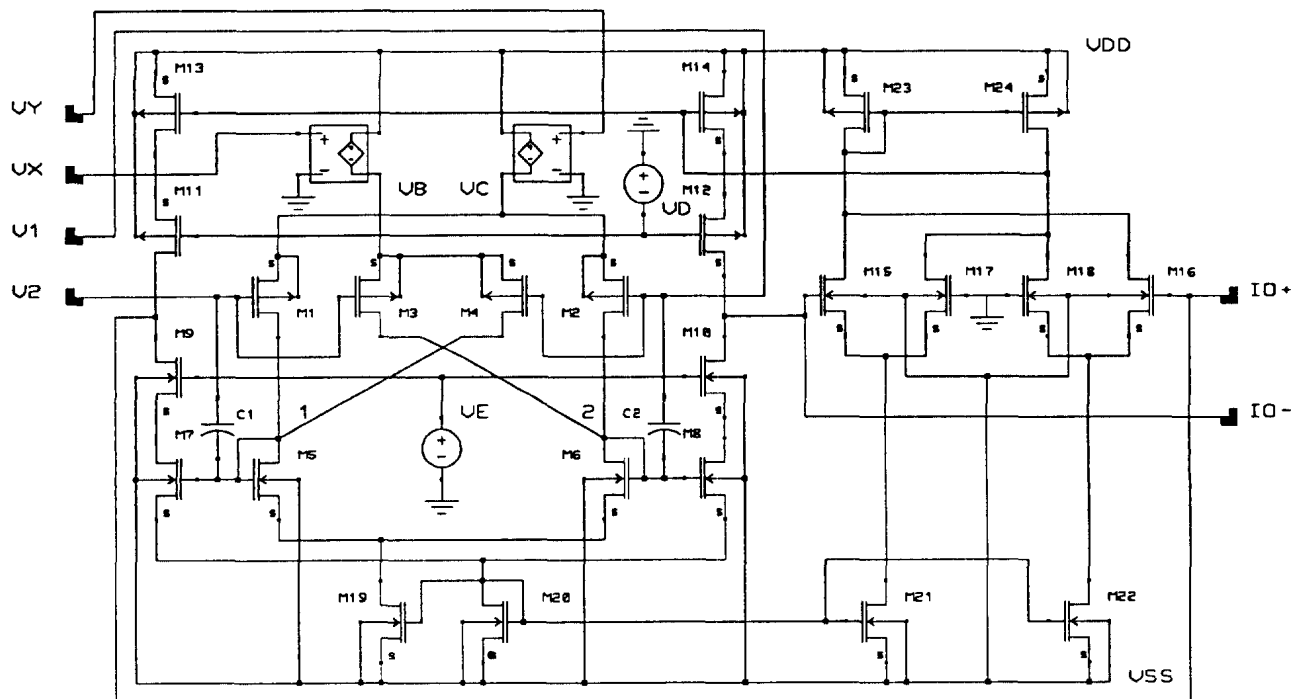


Fig. 1. The circuit diagram of the fully-balanced voltage-tunable CMOS OTA and the differential-difference CMF circuit.

From the above derivation it can be observed that any linear input stage can be used in place of the cross-coupled voltage-controlled quad. Similarly, two and more input stages can be used as in [5] and their currents summed on nodes 1, 2 in Fig. 1. The ultimate advantage of this approach is the short path of the signal from the input stage to the output. Leaving the summing node 1, the signal passes through a diode-connected n-MOS transistor $M5$, which is the reference device in the current mirror $M5, M7$, and through the cascode connected n-type transistor $M9$, but does not travel through the p-type cascode sources $M11 - M13$, which act only as active loads. As the result, neglecting body effect, the dominant pole of the output stage and of the whole OTA can be approximated by

$$p_1 \approx - \frac{g_{m5}}{(C_{gs5} + C_{gs7}) + C_{gd7} (1 + g_{m7}/g_{m9})} \quad (5)$$

which is close to f_T of the minimum sized devices, but decreases with W_7 increasing since C_{gs7}, C_{gd7} and g_{m7} also grow. Eq. (5) reveals how phase tuning in the OTA can be implemented. For this purpose the dc bias voltage V_E is used as in [4] (see Fig. 1). Changes in V_E directly affect C_{gd7} which results in a change of the dominant pole and the phase shift. The electronic phase tuning can be combined with fixed phase compensation using capacitors C_1, C_2 as shown in Fig. 1.

In order to assure wide swing of the output current, the cascode devices are biased on the edge of saturation. The differential output conductance can be expressed by $g_o \approx (g_{ds11} + g_{ds9})/2$. For the parameters in Section IV the differential output resistance r_o is kept in $1 M\Omega$ range.

The output dc level is defined by a differential-difference amplifier [6] as common-mode feedback (CMF) circuit. It retains good linearity and wide bandwidth in connection with very efficient stabilization of the output voltage: changes of the output current in the OTA's whole tuning range do not affect the dc output voltage by more than $5 mV$.

IV. SIMULATION RESULTS

The OTA in Fig. 1 was simulated using SPICE with Level 2 models and $2\mu m$ MOSFETs with $V_{Tn} = 0.745V$, $V_{Tp} = -0.797V$, $k_{on} = 54.4\mu A/V^2$ and $k_{op} = 22.4\mu A/V^2$. All devices in the OTA have the minimum length $L = 2\mu m$. The gate widths W are: $8\mu m$ for $M1 - M4$, $9\mu m$ for $M5 - M6$, $20\mu m$ for $M7 - M8$, $40\mu m$ for $M9 - M10$, $100\mu m$ for $M11 - M12$, $40\mu m$ for $M13 - M14$, $6\mu m$ for $M15 - M18$, $200\mu m$ for $M19 - M20$, $22\mu m$ for $M21 - M22$, $10\mu m$ for $M23 - M24$, $30\mu m$ for $M25 - M26$, $360\mu m$ for $M27$, $30\mu m$ for $M28$, $30\mu m$ for $M29$ and $20\mu m$ for $M30 - M31$. For a power supply of $V_{DD} = -V_{SS} = 5V$, the simulated linearity error

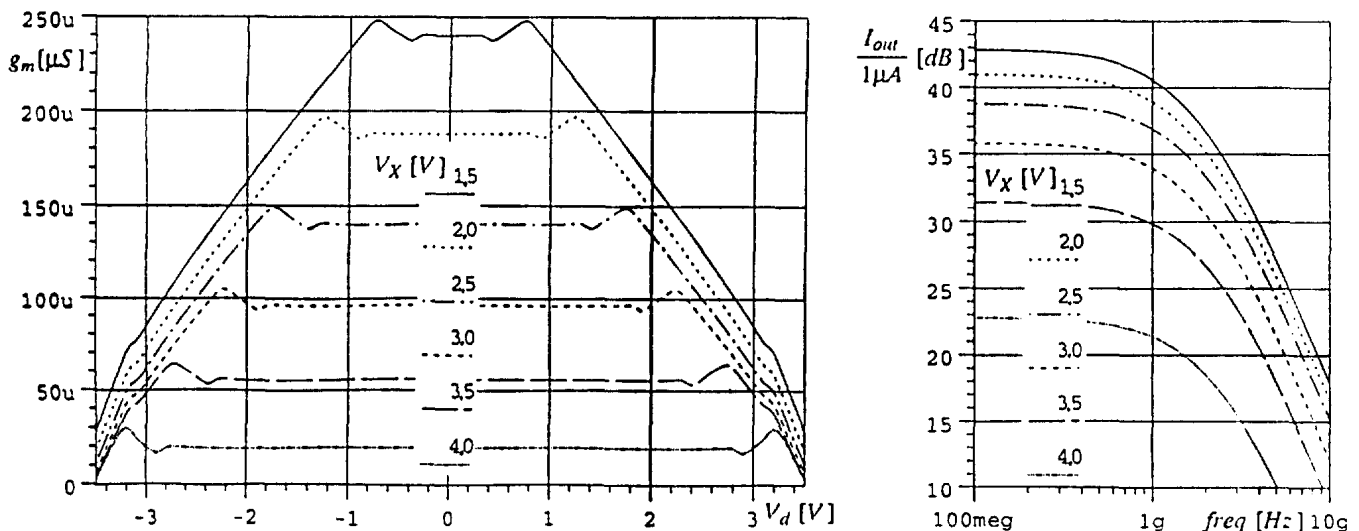


Fig. 3. Performances of the fully-balanced voltage-tunable CMOS OTA in Fig. 1 with the control voltage V_x as parameter and $V_y = 4.3V$,
a) transconductance g_m as the function of the differential input voltage V_d ,
b) frequency response: I_{out} normalized to $1\mu A$.

$$\varepsilon = \frac{I_{out} - g_m(0) V_d}{g_m(0) V_d} 100\% \quad (6)$$

of the OTA in Fig. 1 is as low as 0.052% in the differential input range $\pm 2.5V$, with the control voltage V_X set to 4.0V and $g_m(0)$ being the transconductance for the input voltage $V_d = 0$. When V_X is changed from 4.0V to 1.5V with V_Y fixed at 4.3V, the transconductance g_m varies by a factor of 12, from 16.9 μS to 202 μS (Fig. 3a), the 3dB frequency of the OTA is between 1590MHz and 1226MHz (Fig. 3b), one-sided $PSRR^+$ changes from 55 dB to 70 dB, one-sided $PSRR^-$ varies from 61 dB to 72 dB and for a power supply of $\pm 5V$, the power dissipation is between 39.3mW and 24.7mW. For the 1/f-noise corners of pMOS and nMOS devices equal 10 and 200 kHz respectively, a power supply of $\pm 5V$ and the tuning voltage $V_X = 2.5 V$ the simulated RMS value of the input referred noise $\sqrt{V_{ni}^2}$ integrated over the bandwidth of 1 GHz is 1.967 mV. With $V_{max} = 1.67 V$ corresponding to 0.1% THD the dynamic range (DR) can be calculated as

$$DR = 20 \log \frac{V_{max}}{\sqrt{V_{ni}^2}} \quad (7)$$

and is equal to 58.6 dB. It should be noted that using 1 GHz bandwidth is rather a conservative measure to estimate the DR of a CMOS OTA. A more appropriate approach would be to calculate the DR for an integrator built by loading the above OTA with 1 pF per side. The resulting noise integration bandwidth becomes 37.5 MHz, $\sqrt{V_{ni}^2} = 460 \mu V$ and the DR = 71.2 dB.

V. CONCLUSIONS

A fully-balanced highly-linear high-frequency CMOS OTA has been presented. The idea of the current-coupled cascode output stage results in the superior high-frequency performance of the CMOS OTA circuit operating in the range of GHz - frequencies, available so far only in bipolar or GaAs designs. Both frequency- and Q-tuning are possible, as is necessary for successful design of high-order monolithic analog filters. The simulations

show that the OTA has the potential of giving continuous-time higher-order CMOS filters with cut-off frequencies of 100 MHz and above. The noise performance of the above OTA make possible to design a practical filter with dynamic-range of 60 – 70 dB. The concept of this OTA design lends itself readily for a multiple-input configuration, which can result in substantial savings in the number of required components for a given filter synthesis. Potential use of the OTA as a four-quadrant multiplier has been pointed out.

ACKNOWLEDGMENT

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