For a pMOS input the signal path consists of one p- and three n-devices. In case of a nMOS input, one n- and three p-devices would be present, which would adversely affect the bandwidth of the OTA in Fig. 1.

Assuming that all transistors work in saturation the differential currents of the pairs $M1$, $M2$ and $M3$, $M4$ can be expressed as

$$I_{d1} - I_{d2} = k_p\,(V_{sg1} + V_{sg2} + 2V_{tp})\,(V_{sg1} - V_{sg2}) \quad (1a)$$

$$I_{d4} - I_{d3} = k_p\,(V_{sg4} + V_{sg3} + 2V_{tp})\,(V_{sg4} - V_{sg3}) \quad (1b)$$

where $k_p = 0.5\,\mu_p\,C_{ox}\,(W/L)$ is the transconductance parameter, μ_p, C_{ox}, W and L have their normal meanings and the source-gate voltages are: $V_{sg1} = V_C - V_1$, $V_{sg2} = V_C - V_2$, $V_{sg3} = V_B - V_1$ and $V_{sg4} = V_B - V_2$.

The total differential current I_{in} of the input stage is found as

$$I_{in} = (I_{d1} - I_{d2}) + (I_{d4} - I_{d3}) = 2\,k_p\,V_A\,V_d = g_{in}\,V_d \quad (2)$$

where $V_d = V_{sg1} - V_{sg2} = V_{sg3} - V_{sg4} = V_2 - V_1$ is the differential input voltage, and $V_A = V_C - V_B$ is the control voltage. From (2) it follows that the transconductance of the input stage, $g_{in} = 2\,k_p\,V_A$, can be tuned by varying the tuning voltages V_B and/or V_C. The circuit requires voltage sources V_B and V_C with very low output impedance if the ideal linearity is to be preserved.

By (2) I_{in} and g_{in} depend directly on any change in the tuning voltages V_B and V_C due to variation of V_{DD}. This

Each of them can be seen as a voltage amplifier working in a unity-gain configuration with its negative input terminal connected to V_X and the positive input terminal connected to V_B. Transistor $M29$ works in feedback configuration with its gate driven form the output of the amplifier and its source tied up to the input positive terminal and provides the current drive necessary to achieve low output impedance. V_B is forced to closely track V_X because the input nodes of a voltage amplifier form a "virtual ground". Since the *dc* voltage of the gate of $M29$ is taken form the drains of $M26$, $M28$, the output voltage is nearly independent of variations in V_{DD}. The resulting one-sided $PSRR^+$ is better than $55dB$. Naturally, the differential $PSRR^+$ even when limited by device mismatches will be much higher than this value. In a practical realization of a filter the sources V_B and V_C can be shared by all OTAs. Note that the circuit can act as a four-quadrant multiplier for differential input signals with $I_{in} = 2\,k_p\,\alpha\,(V_Y - V_X)\,(V_2 - V_1)$, because $V_B = \alpha\,V_X$ and $V_C = \alpha\,V_Y$, where $\alpha \approx 1$ is the gain of the two sources.

III. THE OUTPUT STAGE

An output stage with very good linearity, high output impedance and wide bandwidth is obtained from an adaptation of the bipolar approach used in [4] which seems to be a general method for building fast OTAs. The main difference between the two circuits consists in placing the mirror diodes $M5$, $M6$ at the drains of the input quad $M1 - M4$ rather than at the emitters of the input pair as in case of [4]. This improvement is possible because the complementary device is available in CMOS and since common-source configuration has better noise performance than a follower, it results in a lower noise level.

From the above derivation it can be observed that *any* linear input stage can be used in place of the cross-coupled voltage-controlled quad. Similarly, two and more input stages can be used as in [5] and their currents summed on nodes 1, 2 in Fig. 1. The ultimate advantage of this approach is the short path of the signal from the input stage to the output. Leaving the summing node 1, the signal passes through a diode-connected n-MOS transistor $M5$, which is the reference device in the current mirror $M5, M7$, and through the cascode connected n-type transistor $M9$, but does not travel through the p-type cascode sources $M11 - M13$, which act only as active loads. As the result, neglecting body effect, the dominant pole of the output stage and of the whole OTA can be approximated by

$$p_1 \approx -\frac{g_{m5}}{(C_{gs5} + C_{gs7}) + C_{gd7}\,(1 + g_{m7}/g_{m9})} \qquad (5)$$

which is close to f_T of the minimum sized devices, but decreases with W_7 increasing since C_{gs7}, C_{gd7} and g_{m7} also grow. Eq. (5) reveals how phase tuning in the OTA can be implemented. For this purpose the *dc* bias voltage V_E is used as in [4] (see Fig. 1). Changes in V_E directly affect C_{gd7} which results in a change of the dominant pole and the phase shift. The electronic phase tuning can be combined with fixed phase compensation using capacitors C_1, C_2 as shown in Fig. 1.

In order to assure wide swing of the output current, the cascode devices are biased on the edge of saturation. The differential output conductance can be expressed by $g_o \approx (g_{ds11} + g_{ds9})/2$. For the parameters in Section IV the differential output resistance r_o is kept in 1 $M\Omega$ range.

The output *dc* level is defined by a differential-difference amplifier [6] as common-mode feedback (CMF) circuit. It retains good linearity and wide bandwidth in connection with very efficient stabilization of the output voltage: changes of the output current in the OTA's whole tuning range do not affect the *dc* output voltage by more than 5 *mV*.

IV. SIMULATION RESULTS

The OTA in Fig. 1 was simulated using SPICE with Level 2 models and 2μm MOSFETs with $V_{Tn} = 0.745V$, $V_{Tp} = -0.797V$, $k_{on} = 54.4\mu A/V^2$ and $k_{op} = 22.4\mu A/V^2$. All devices in the OTA have the minimum length $L = 2\,\mu m$. The gate widths W are: 8μm for $M1 - M4$, 9μm for $M5 - M6$, 20μm for $M7 - M8$, 40μm for $M9 - M10$, 100μm for $M11 - M12$, 40μm for $M13 - M14$, 6μm for $M15 - M18$, 200μm for $M19 - M20$, 22μm for $M21 - M22$, 10μm for $M23 - M24$, 30μm for $M25 - M26$, 360μm for $M27$, 30μm for $M28$, 30μm for $M29$ and 20μm for $M30 - M31$. For a power supply of $V_{DD} = -V_{SS} = 5V$, the simulated linearity error

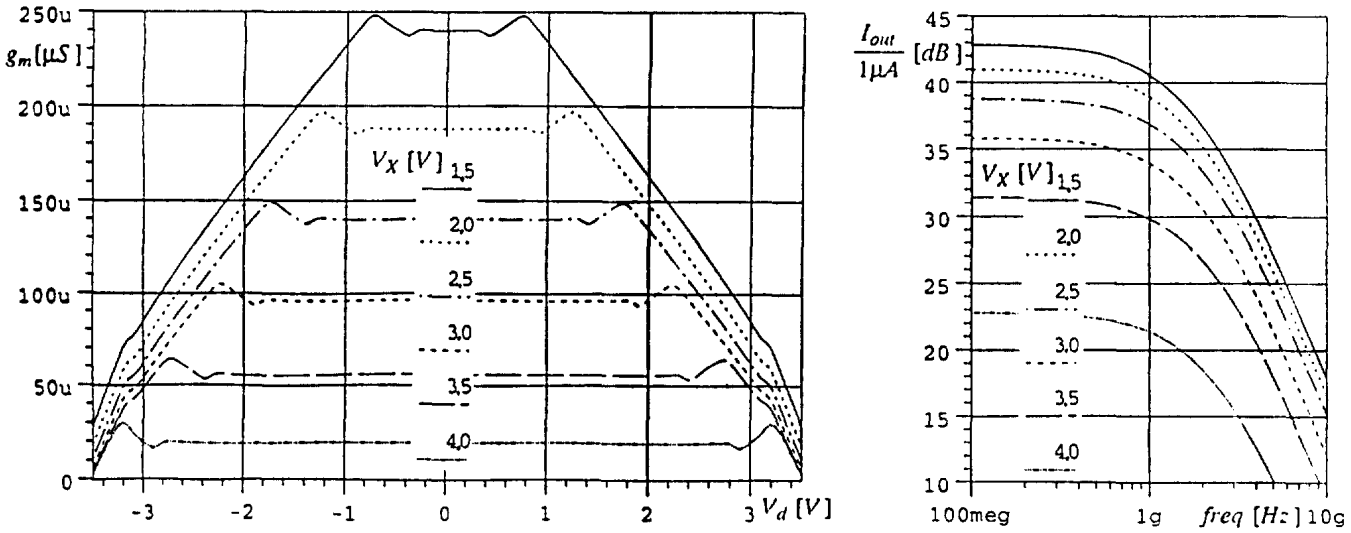

Fig. 3. Performances of the fully-balanced voltage-tunable CMOS OTA in Fig. 1 with the control voltage V_X as parameter and $V_Y = 4.3V$,
a) transconductance g_m as the function of the differential input voltage V_d,
b) frequency response: I_{out} normalized to 1μA.

$$\varepsilon = \frac{I_{out} - g_m(0)\, V_d}{g_m(0)\, V_d}\, 100\% \qquad (6)$$

of the OTA in Fig. 1 is as low as 0.052% in the differential input range $\pm 2.5V$, with the control voltage V_X set to $4.0V$ and $g_m(0)$ being the transconductance for the input voltage $V_d = 0$. When V_X is changed from $4.0V$ to $1.5V$ with V_Y fixed at $4.3V$, the transconductance g_m varies by a factor of 12, from $16.9\mu S$ to $202\mu S$ (Fig. 3a), the $3dB$ frequency of the OTA is between $1590MHz$ and $1226MHz$ (Fig. 3b), one-sided $PSRR^+$ changes from 55 dB to 70 dB, one-sided $PSRR^-$ varies form 61 dB to 72 dB and for a power supply of $\pm 5V$, the power dissipation is between $39.3mW$ and $24.7mW$. For the 1/f-noise corners of pMOS and nMOS devices equal 10 and 200 kHz respectively, a power supply of $\pm 5V$ and the tuning voltage $V_X = 2.5\ V$ the simulated RMS value of the input referred noise $\sqrt{\overline{V^2_{ni}}}$ integrated over the bandwidth of $1\ GHz$ is $1.967\ mV$. With $V_{max} = 1.67\ V$ corresponding to 0.1% THD the dynamic range (DR) can be calculated as

$$DR = 20 \log \frac{V_{max}}{\sqrt{\overline{V^2_{ni}}}} \qquad (7)$$

and is equal to $58.6\ dB$. It should be noted that using $1\ GHz$ bandwidth is rather a conservative measure to estimate the DR of a CMOS OTA. A more appropriate approach would be to calculate the DR for an integrator built by loading the above OTA with $1\ pF$ per side. The resulting noise integration bandwidth becomes $37.5\ MHz$, $\sqrt{\overline{V^2_{ni}}} = 460\ \mu V$ and the $DR = 71.2\ dB$.

V. CONCLUSIONS

A fully-balanced highly-linear high-frequency CMOS OTA has been presented. The idea of the current-coupled cascode output stage results in the superior high-frequency performance of the CMOS OTA circuit operating in the range of GHz - frequencies, available so far only in bipolar or GaAs designs. Both frequency- and Q-tuning are possible, as is necessary for successful design of high-order monolithic analog filters. The simulations show that the OTA has the potential of giving continuous-time higher-order CMOS filters with cut-off frequencies of 100 MHz and above. The noise performance of the above OTA make possible to design a practical filter with dynamic-range of $60 - 70\ dB$. The concept of this OTA design lends itself readily for a multiple-input configuration, which can result in substantial savings in the number of required components for a given filter synthesis. Potential use of the OTA as a four-quadrant multiplier has been pointed out.

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