Frequency and Phase Tuning of Continuous-Time Integrated Filters Using Common-Mode Signals

Adam Wyszyński and Rolf Schaumann
Department of Electrical Engineering, Portland State University
Portland, Oregon 97207-0751, U.S.A.
tel. (503) 725-3806, e-mail adamw@ee.pdx.edu

ABSTRACT

A system for frequency- and Q-factor tuning resulting in a self-tuned filter is proposed. The method uses a common-mode (CM) signal as reference. No Master filter is required since CM reference signals are directly applied to the main filter built as two separate but identical single-ended paths. Since the two filters are built as cascade designs the tuning signal can be conveniently applied to the inputs of the two highest-Q biquads. By summing the outputs of these biquads the differential signals cancel and the resulting CM tuning signal is used in classical frequency- and Q-tuning schemes. CM tuning signals are rejected at the output of the filter by a differential buffer. For a monolithic realization, a 7th-order equiripple delay filter with cut-off frequency tunable from 5 MHz to 40 MHz and the maximum Q of 2 has been selected. It is built with a single-ended double-input CMOS triode transconductor (G_M) and a "lossy biquad" which requires no common-mode feedback (CMF) circuitry. The filter operates from a single 5 V power supply and dissipates 200 mW. The simulated signal-to-noise (S/N) ratio equals 70 dB for an input range of 1 V_{pp}. The advantages of the proposed approach include on-line tuning, simpler circuitry by eliminating the Master filters and CMF circuits as well as reduced power, noise and die area.

I. INTRODUCTION

Due to unavoidable process tolerances continuous-time integrated filters need to be tuned as their frequency parameters are set by g_m/C ratios. Similarly, phase shifts of transconductance amplifiers need to be compensated even for moderate values of Q, such as $Q=2$, if filter specifications are to be realized correctly [1]. This becomes particularly important in high-Q filters where the effects of phase shifts for a transfer function are very detrimental and may lead to instability of a filter.

Both frequency- and Q-tuning should be performed when the filter is in operation, i.e., with the main signal applied. As a consequence, Master-Slave (M-S) tuning schemes have been postulated [1]-[5], in which errors in frequency and Q of a Master (M) designed as a partial replica of the main filter (the Slave (S)) are measured and corrections are applied both to M and S. Among the disadvantages of an M-S method are additional noise, die area, power consumption and that the errors are measured in a filter which is different from the tuned one. The accuracy of the M-S method is as good as matching between M and S which is limited by on-chip component matching and, especially, by simplifications of the M structure compared to S.

Ideally, M and S should be one and the same filter, i.e., the signal and the reference should be applied simultaneously. Unfortunately, because reference signals may not appear at the filter output nor the main signal at the reference output, the ideal situation has not been considered possible. The proposed method, shown in Fig. 1, makes the attractive concept of an on-line continuously self-tuned filter feasible by providing a scheme wherein reference and main signals are applied simultaneously to the filter but are readily separated at the outputs. It is assumed that the filter blocks $H(s)$ are linear.

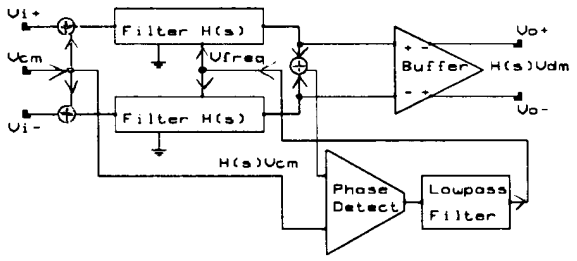

Fig. 1. The idea of a self-tuned frequency tuning scheme using a CM reference.

An architecture is proposed where the reference is not seen at the main signal output and the main signal is not seen at the tuning output. There is no need for separate M and S; rather M and S are the same. As described in Section III, the reference signals are applied directly to S as common-mode (CM) signals and rejected at the output.

II. THE BUILDING BLOCKS

The selected filter structure for CM tuning uses single-ended cascade designs. One advantage of this approach is that a biquad is a convenient block for measuring frequency and Q errors; also it avoids common-mode feedback (CMF) circuits, resulting from the fact that a biquad is naturally lossy. The biquads should be designed so that the transfer functions for differential-mode (DM) and CM signals are the same.

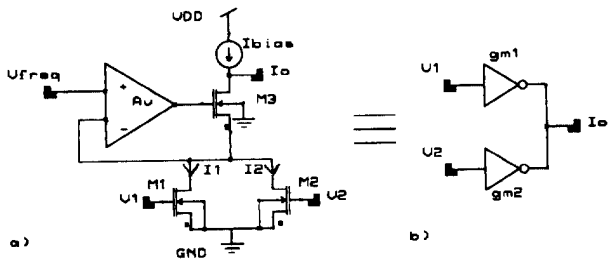

Fig. 2. CMOS triode-region double-input single-ended transconductor (G_M): a) schematic, b) block diagram.

The simplified stage [8] in Fig. 2 is a double-input single-ended linear transconductor G_M. Its output current I_o is the sum of drain currents of the MOSFET resistors M_1, M_2 into the low-impedance source of M_3. Using a double-input G_M substantially simplifies the filter circuitry since rather than repeating the whole transconductor with the associated voltage amplifier A_V, a single input device is added [9]. Because M_1, M_2 are MOSFET resistors, voltage-to-current conversion is linear even in the single-ended G_M. Thereby, the single-ended filters built out of this G_M are also linear. The circuit realizes

$$I_o = -g_{m1}V_1 - g_{m2}V_2 \qquad (1)$$

where

$$g_{mi} = \partial i_{Di}/\partial v_i = \mu_n C_{ox} (W/L)_i V_{DS} \qquad i = 1,2 \quad (2)$$

Tunability is obtained by changing the drain-source voltage using transistor M_3 in connection with a voltage amplifier A_V. The purpose of this amplifier is to improve the linearity of G_M by boosting g_{m3} and to increase the output impedance of the transconductor. Differential structures consisting of two such stages and CMF are possible. They are not appropriate for the proposed CM tuning scheme as they suppress CM signals and result in different CM and DM transfer functions.

Note that the *dc* output voltage of the G_M in Fig. 2 needs to be defined since it is at the node between two high-impedance current sources. Instead of using a CMF circuit, a technique of defining the output voltage by active loading of the output of each transconductor by a $1/g_m$ resistor has been postulated, using precise biasing and synthesising the biquads from lossy integrators [10]. The lossy g_m–C–$1/g_m$ integrators and "lossy biquads" are shown in Fig. 3.

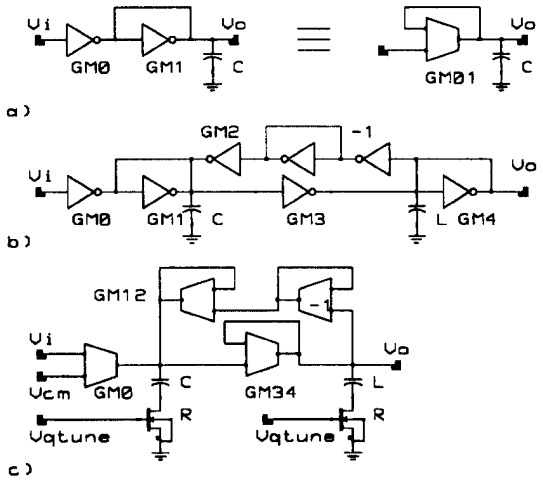

Fig. 3. The lossy integrator-based building blocks:
a) g_m–C–$1/g_m$ integrators based on single- and double-input G_M's,
b) "lossy" biquad based on single-input G_M,
c) "lossy" biquad based on double-input G_M with phase compensation MOSFETs and a CM reference input.

They realize

$$\frac{V_o}{V_i} = \frac{-g_{m0}}{g_{m1} + sC} \qquad (3)$$

$$\frac{V_o}{V_i} = \frac{g_{m0}g_{m3}}{g_{m1}g_{m4} + g_{m2}g_{m3} + s(g_{m1}L + g_{m4}C) + s^2LC}$$

Note that both L and C are capacitors. In order to maintain a single signal path from the input to the output, the biquads in Fig. 3 must contain their own inversion block ("-1") which results in an additional internal node not loaded by a circuit capacitor. Due to parasitic C, the presence of such a node increases the total phase shift but since the resulting phase error can be fully compensated by MOSFET resistors controlled by a Q-tuning scheme (Fig. 3c) the effect is not critical for this application. Further required building blocks are an input single-ended to differential converter (necessary if the input is single-ended) and an output differential to single-ended or differential-in differential-out (in case the output must be differential) high common-mode rejection (CMR) buffer.

III. THE METHOD

Based on the proposed method, a seventh-order equiripple delay filter with cut-off frequency tunable from 5 *MHz* to 40 *MHz* and the highest Q of 2 has been designed in a standard 2 μ *m* CMOS technology. It is a cascade design with two identical single-ended filters as shown in Fig. 4 using the lossy g_m–C–$1/g_m$ integrators and "lossy biquads" of Fig. 3 requiring no CMF circuit.

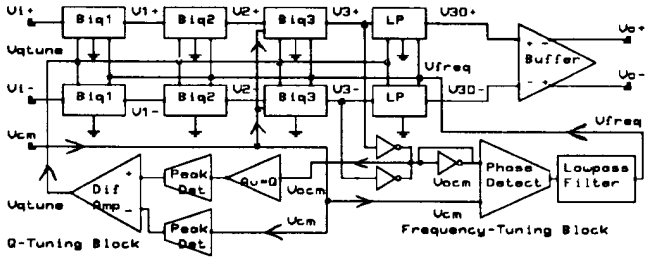

Fig. 4. The schematic of a 7-th order cascade filter self- tuned by CM signals with frequency and Q tuning loops.

The tuning reference signal V_{CM} is entered into the signal path of the filter as CM. It is applied to the second inputs of g_{m0} in Fig. 3c at two highest–Q biquads (Biq3) in Fig. 4. After passing through these biquads and the first-order sections (LP) the reference CM signals are rejected by a high CMR differential buffer. The output reference CM signals are obtained by summing the outputs of the highest–Q biquads as shown in Fig. 4. It can be performed by a double-input G_M loaded with a $1/g_m$ resistor. Assuming that both single-ended biquads are linear and matched, the output signals can be calculated as follows

$$V_3^+ = H_3^+(s)\,(V_2^+ + V_{CM}) \qquad (4)$$
$$V_3^- = H_3^-(s)\,(V_2^- + V_{CM})$$

where $H_3^+(s) \approx H_3^-(s) = H_3(s)$ are the transfer functions of the two biquads. After summing the signals, assuming that $1/2\,V_{DM} = V_2^+ = -V_2^-$ the CM tuning signal is extracted as

$$V_{OCM} = -(V_3^+ + V_3^-) \qquad (5)$$
$$= -1/2\,[H_3^+(s) - H_3^-(s)]\,V_{DM} - [H_3^+(s) + H_3^-(s)]\,V_{CM}$$
$$= -1/2\,\Delta H_3(s)\,V_{DM} - 2\,H_3(s)\,V_{CM}$$

Summing causes the differential signals to cancel out if the two biquads are well matched so that only CM test signals are processed by the tuning circuitry. The small possible interference of differential signals caused by unavoidable mismatches should not have a critical impact on the accuracy of tuning scheme. The tuning signal can be processed by a frequency tuning scheme [3], [5], [7], shown in Fig. 4, consisting of a CM-frequency voltage reference, a phase detector and a lowpass filter. The CM tuning signal passing through the biquad (Biq3) is compared with the CM reference by the phase detector. Both signals are kept in quadrature as the output of the phase detector is lowpass filtered and applied as the input voltage V_{freq} to the g_m setting amplifiers A_V (Fig. 2) controlling V_{DS} of the MOSFET resistors (2).

The Q–factor is adjusted using the same CM tuning signal by an amplitude locking loop [5]-[7] (Fig. 4) consisting of a reference amplifier, two peak detectors and a differential amplifier. The CM tuning signal is amplified by the biquad (Biq3) at its resonance frequency to approximately Q-times the reference. If the reference amplifier has its gain set to be equal to Q, the differential amplifier adjusts the voltage V_{qtune} at the gates of MOSFET resistors in series with integration capacitors (Fig. 3c) such that phase and Q are correct. The MOSFET resistors are introducing a phase-leading zero to the frequency response, compensating for the phase-lag due to the poles of the G_M stage. An advantage of the described method is that the reference frequency can be chosen where the tuning scheme has the highest sensitivity: at the resonance frequency of the highest–Q biquad. In the filter, the CM signal is further attenuated by the trailing first-order section (LP); in addition the pole frequency of the highest–Q biquad falls into the stopband of the filter where residual CM components are of less concern.

As mentioned previously, the output of the filter is obtained by taking the difference of the output signals of both sides by a differential buffer. Note that in principle there is no need for a separate buffer as the trailing first-order section could perform this function resulting in lowered chip area, power consumption, distortion and noise levels. If the buffer is as linear as the rest of the filter and if it has a high CMR in the operational range of the filter, the basic limitation imposed on the filter's dynamic range are mismatches between the transfer functions $H_{3O}^+(s) \approx H_{3O}^-(s) \approx H_{3O}(s)$ from the input of the CM reference signal to the filter output. The output can be calculated as

$$V_O = V_{3O}^+ - V_{3O}^- \qquad (6)$$
$$= [H_{3O}^+(s) - H_{3O}^-(s)]\,V_{CM}$$
$$+ H_{3O}^+(s)\,V_2^+ - H_{3O}^-(s)\,V_2^-$$
$$= \Delta H_{3O}(s)\,V_{CM} + 1/2\,H_{3O}(s)\,V_{DM}$$

Note that the output can be single-ended or differential

but in both cases CM signals are rejected and Eq. 6 applies. If the matching between both sides was accurate to 0.3 %, the dynamic range would be 50 *dB* provided the DM and CM signals were the same. Since the tuning scheme can operate with CM signals as low as several tens of *mV* and assuming that the DM signal is 1 *V*, this theoretical S/N ratio can be as high as 80 *dB*. This value depends on the quality of DM rejection of the summers at the output of Biq. 3. Also, the theoretical S/N ratio has to be modified by the CMR value of the output buffer. Its CMR should be as high as 50 *dB* at the pole frequency of the highest–Q biquad if the theoretical S/N is to be preserved. Ultimately, the S/N ratio is set by the filter noise depending on the total power dissipated and the total capacitance used.

IV. CONCLUSIONS

A tuning method for self-tuned continuous-time integrated filters using CM signals has been proposed. It uses a CM reference signal and is able to operate while the main signal is applied. The additional advantages expected from this approach include simpler circuitry due to elimination of Master filters in frequency- and Q–tuning schemes as well as all CMF circuits. This in turn results in reduced power, noise and die area.

Provided CMR of the differential buffer taking the difference of the signals of both sides of filter is sufficiently high, the CM reference signals cancel out and the output signal contains only the differential component with a small residual CM noise due to finite CMR of the differential buffer. Although the filter output may be single-ended, the whole signal processing is of a differential nature implying the usual 6 *dB* gain in dynamic range and cancellation of all even harmonics, giving the filter reduced distortion.

Special care should be taken during the layout stage if good matching between biquads that is necessary for cancellation of the CM signal is to be achieved. The described method is particularly suitable for cascade designs but it can be extended for other types of filters. For a 2 μm CMOS MOSIS process using a single 5 *V* power supply the simulated power dissipation of a filter without the tuning scheme is of the order of 200 *mW*, the simulated THD is 0.7 % for 1.0 *Vpp* @ 5 *MHz*, the simulated input referred noise is 225 μV for 100 *MHz* bandwidth which yields the S/N = 70 *dB*.

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