Avoiding Common-Mode Feedback in Continuous-Time $g_m - C$ Filters by Use of Lossy Integrators

Adam Wyszyński and Rolf Schaumann
Department of Electrical Engineering, Portland State University
Portland, Oregon 97207-0751, U.S.A.
tel. (503) 725-3806, e-mail adamw@ee.pdx.edu

ABSTRACT

A method of continuous-time fully-differential signal processing is proposed which avoids the use of common-mode feedback (CMF) circuitry. Instead, the *dc* output voltage of transconductors (G_M's) is defined by a $1/g_m$

DMO AISP [4]-[6]. Additional problems are related to limiting power consumption, die area and the noise generated by CMF circuitry.

Having pointed out the deficiencies of CMF, a circuit solution is proposed that totally avoids CMF circuitry. As the output resistance of G_M which is formed by a parallel connection of the output resistances of the p- and n-sides of G_M and the input resistance of the CMF circuit. C_0 is basically formed by the integration capacitor augmented by the output capacitance of G_M and the input capacitance of the CMF circuit.

Calculating the CM voltage $V_e = V_{cm} + V_f$ with the CMF loop closed, where V_{cm} is the original CM signal at the output of G_M, $V_f = g_{m0} Z_0 V_1$ with $V_1 = -g_{m1} Z_1 V_e$, is the signal fed back by the CMF circuit, and $Z_0 = R_0/(1 + s\tau_0)$, $Z_1 = R_1/(1 + s\tau_1)$ where $\tau_0 = R_0 C_0$, $\tau_1 = R_1 C_1$, results in:

$$V_e = \frac{V_{cm}}{1 + g_{m0} g_{m1} Z_0 Z_1} = \frac{V_{cm}}{1 + T/[(1 + s\tau_0)(1 + s\tau_1)]} \quad (1)$$

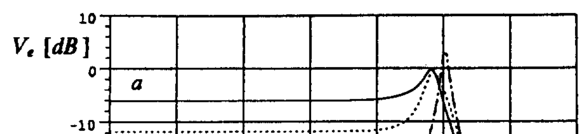
which, assuming that the dc loop gain $T = g_{m0} g_{m1} R_0 R_1 \gg 1$, can be simplified to

$$V_e = \frac{V_{cm}}{T} \frac{(1 + s\tau_0)(1 + s\tau_1)}{1 + s(\tau_0 + \tau_1)/T + s^2 (C_0 C_1)/(g_{m0} g_{m1})} \quad (2)$$

From (2) it can be seen that V_{cm} as expected is suppressed by factor T, and that the frequency response of the CMF loop in Fig. 1b can be simplified to have two real left-hand plane zeros $1/\tau_0$ and $1/\tau_1$ and two complex poles with pole frequency ω_o and quality-factor Q given by

$$\omega_o = \sqrt{g_{m0} g_{m1}/(C_0 C_1)} \qquad Q = \sqrt{T \tau_0 \tau_1}/(\tau_0 + \tau_1) \quad (3)$$

The simulated frequency response for three types of CMF circuit [1]-[3] is shown in Fig. 2.



tunately, in most practical CMF circuits the peaking occurs in the operating range of a DMO AISP system, i.e., in the range of $10 - 200\,MHz$. Thereby, at high-frequencies a CMF loop loses its attenuation for the CM signals while still generating noise and distortion. From (3) it follows that Q of the pair of complex poles in the denominator of (2) is proportional to $\sqrt{T}$: the more dc "stabilization" is required from a CMF loop the higher a Q results.

On the other hand, it can be seen from (3) that increasing C_0, C_1 or decreasing R_0, R_1 results in lowering Q, which indicates a natural way of stabilizing a CMF loop. In such a case, the loop loses its attenuation even earlier due to the zeros moving to lower frequencies. Since the g_m-values of the CM-detector and the load current source have in practice additional phase shift due to their higher-order poles, this contribution can be modeled by $g_m(s) \approx g_{m0}(1 - s/p)$. The additional phase shift introduced into the CMF loop causes the enhanced Q to be $Q^* \approx Q/[1 - 2Q(\omega_o/p)]$ which can be derived from (3) assuming for simplicity that $g_{m0}/C_0 \approx g_{m1}/C_1$. From Q^* it follows that, e.g., for phase shifts as small as $0.1\,rad \approx 6^o$, with $Q = 5$ corresponding to T in the range of $30 - 40\,dB$, the CMF loop may become unstable. From the above analysis it can be seen that CMF circuitry can be very detrimental to the AISP system performance. Therefore, a preferred solution is to avoid the use of CMF circuitry entirely.

III. DEFINING DC OUTPUT VOLTAGE WITH $1/G_M$

A simple method of avoiding a CMF circuit is to load the output of a G_M-cell with a resistor. Thereby, the dc output voltage is defined and there is no need for CMF circuitry.

tial structures is achieved readily by using two single-ended filters in parallel and driving them differentially as in Fig. 6.

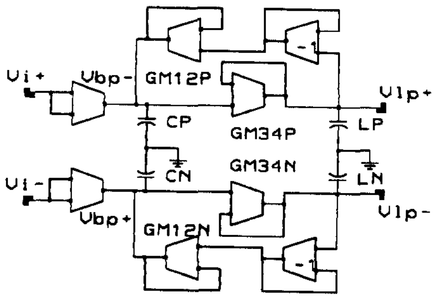


Fig. 6. The differential "lossy biquad" built with double-input G_M's.

Note that because of the nature of V-I conversion the single-ended G_M in Fig. 3b is linear; so is any single-ended filter built with such G_M-cells. The differential structures further improve the linearity by cancelling all even harmonics as well as power supply or CM noise.

IV. CONCLUSIONS

A method of avoiding CMF circuitry in continuous-time g_m-C filters has been proposed. The drawbacks of CMF circuitry, including poor high-frequency performance, problems with stability, as well as associated additional power, die area, distortion and noise, have been pointed out. The *dc* output voltages in the method presented are defined by use of lossy integrators in connection with a precise biasing scheme. The accuracy of setting the *dc* output voltage for 10:1 tuning range of g_m is demonstrated in Table 1.

Table 1. Output dc Voltage Variation for $V_{DD} = 5\ V$

V_{TUNE}	I_B	g_m	V_{BP}	V_{LP}
1250 mV	145 uA	51 uS	2475 mV	2513mV
1500 mV	704 uA	270 uS	2498 mV	2500mV
1750 mV	1159 uA	496 uS	2501 mV	2497mV

An active g_m-C filter synthesis method using lossy g_M-C-$1/g_m$ integrators has been demonstrated. The expected advantages of this approach for the design of integrated fully-differential continuous-time filters include simpler circuitry due to elimination of all CMF circuits, improved stability, reduced power, die area, distortion and noise. The described approach is naturally suited to lowpass cascade filters but other filter structures are being also investigated.

ACKNOWLEDGMENT

This work was supported in part by the 1992/1993 Tektronix grant, and the NSF under grant No. MIP 91-21360.

REFERENCES

[1] T. Choi, *et al.*, "High-Frequency CMOS Switched-Capacitor Filters for Communications Applications," *IEEE J. Solid-State Circ.*, vol. SC-18., pp. 652-664, 1983

[2] P. W. Li, *et al.*,, "A Ratio-Independent Algorithmic Analog-to-Digital Conversion Technique," *IEEE J. Solid-State Circuits*, vol. SC-19., pp. 828-836, 1984

[3] R. A. Whatly, "Fully Differential Operational Amplifier with DC Common-Mode Feedback," U.S. Patent 4 573 020, Feb. 25, 1986

[4] P. Van Peteghem and J. Duque-Carrillo, "A General Description of Common-Mode Feedback in Fully Integrated Amplifiers," *Proc. IEEE Int. Symp. Circ. Syst.*, pp. 3209 - 3212, 1990

[5] J. F. Duque-Carrillo, "Control of the Common-Mode Component in CMOS Continuous-Time Fully-Differential Signal Processing," Kluwer, *Analog ICs and Signal Proc. J.*, vol. 4, no. 2, pp. 131-140, 1993

[6] A. Wyszyński, R. Schaumann, S. Szczepański, and P. Van Halen, "Design of a 2.7 GHz linear OTA and a 250 MHz Elliptic Filter in Bipolar Transistor-Array Technology," *IEEE Trans. Circ. Syst. Part II*, CAS-40, no. 1, pp. 19 - 31, 1993

[7] S. Takagi, *et al.*, "100-MHz Monolithic Low-Pass Filters With Transmission Zeros Using NIC Integrators," *IEEE J. Solid-State Circ.*, vol. SC-26. no. 4, pp. 669-671, 1991

[8] G. A. DeVeirman and R. Yamasaki, "Design of Bipolar 10-MHz Programmable Continuous Time 0.05^0 Equiripple Linear Phase Filter," *IEEE J. Solid-State Circ.*, vol. SC-27. no. 3, pp. 324-331, 1992

[9] A. Wyszyński, "Low-Voltage CMOS and BiCMOS Triode Transconductors and Integrators with Gain-Enhanced Linearity and Output Impedance," *Elect. Lett.*, vol. 30, 1994

[10] A. Wyszyński and R. Schaumann, "Frequency and Phase Tuning of Continuous-Time Integrated Filters Using Common-Mode Signals," *Proc. IEEE Int. Symp. Circ. Syst.*, London, 1994