Avoiding Common-Mode Feedback in Continuous-Time g_m–C Filters by Use of Lossy Integrators

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ABSTRACT

A method of continuous-time fully-differential signal processing is proposed which avoids the use of common-mode feedback (CMF) circuitry. Instead, the *dc* output voltage of transconductors (G_M's) is defined by a $1/g_m$ resistor load and by implementing a precise biasing scheme to control the *dc* output voltage with accuracy similar to that of a good CMF circuit. The approach results in single-ended cascade filters built around a single-ended double-input CMOS triode-region G_M. Fully differential filters are obtained by connecting two such single-ended structures in parallel and driving them with differential signals. The advantages of the discussed method result in systems with improved stability, and reduced noise, distortion, power consumption and the area.

I. INTRODUCTION

With power supply and transistor dimensions constantly decreasing, precision and a sufficient dynamic range (DR) of an analog integrated signal processing (AISP) system can be maintained by a fully differential mode of operation (DMO). In order to implement a DMO AISP system, an additional common-mode feedback (CMF) loop stabilizing the *dc* output voltage level is mandatory. It is due to the fact that the output impedance of a transconductor (G_M) is high (ideally ∞); thus, any variation in the CM *dc* current at the output causes the *dc* output voltage to shift so that the output devices of G_M may leave the linear range of operation. The discussion of CMF loop *ac* performance and the stability issue will be presented in Section II.

In recent years only few distinctly different CMF schemes have been reported [1]-[5]. Much more attention was devoted to the design of differential-mode (DM) signal amplifiers. Unfortunately, the performance of an DMO AISP system depends equally on the performance of the DM and CM parts. In particular, a CMF circuit should be as linear as the DMO AISP system and it should maintain the suppression of CM components in the whole band of DMO AISP [4]-[6]. Additional problems are related to limiting power consumption, die area and the noise generated by CMF circuitry.

Having pointed out the deficiencies of CMF, a circuit solution is proposed that totally avoids CMF circuitry. As discussed in Section III, the *dc* output voltage of a transconductor G_M is defined by loading it with a $1/g_m$ resistor and using a precise biasing scheme. Simultaneously, a system technique has been proposed to synthesize a certain class of filters by use of lossy integrators. The approach discussed in Section IV results in cascade filters built around a "lossy biquad" which does not require a CMF circuit.

II. *AC* PERFORMANCE OF A CMF LOOP

An *ac* model of a CMF circuit in its basic form in Fig. 1 is a two-stage voltage amplifier and as such may have problems with stability unless properly designed and compensated.

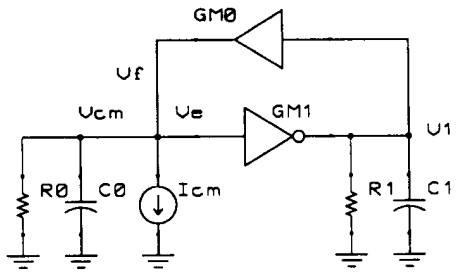

Fig. 1. The *ac* model of a typical CMF scheme

The CMF circuit configurations in [1]-[6] follow the same generic *ac* pattern resulting in a frequency response typical of a CMF loop. The *ac* model shown in Fig. 1 consists of a CM-detector g_{m1} loaded with R_1 and C_1. These components are formed as the sum of the output impedance of g_{m1} and the input impedance of the following load current source, g_{m0}. In a g_m–C integrator, R_0 is

the output resistance of G_M which is formed by a parallel connection of the output resistances of the p- and n-sides of G_M and the input resistance of the CMF circuit. C_0 is basically formed by the integration capacitor augmented by the output capacitance of G_M and the input capacitance of the CMF circuit.

Calculating the CM voltage $V_e = V_{cm} + V_f$ with the CMF loop closed, where V_{cm} is the original CM signal at the output of G_M, $V_f = g_{m0} Z_0 V_1$ with $V_1 = -g_{m1} Z_1 V_e$, is the signal fed back by the CMF circuit, and $Z_0 = R_0/(1 + s\tau_0)$, $Z_1 = R_1/(1 + s\tau_1)$ where $\tau_0 = R_0 C_0$, $\tau_1 = R_1 C_1$, results in:

$$V_e = \frac{V_{cm}}{1 + g_{m0} g_{m1} Z_0 Z_1} = \frac{V_{cm}}{1 + T/[(1 + s\tau_0)(1 + s\tau_1)]} \quad (1)$$

which, assuming that the dc loop gain $T = g_{m0} g_{m1} R_0 R_1 \gg 1$, can be simplified to

$$V_e = \frac{V_{cm}}{T} \frac{(1 + s\tau_0)(1 + s\tau_1)}{1 + s(\tau_0 + \tau_1)/T + s^2 (C_0 C_1)/(g_{m0} g_{m1})} \quad (2)$$

From (2) it can be seen that V_{cm} as expected is suppressed by factor T, and that the frequency response of the CMF loop in Fig. 1b can be simplified to have two real left-hand plane zeros $1/\tau_0$ and $1/\tau_1$ and two complex poles with pole frequency ω_o and quality-factor Q given by

$$\omega_o = \sqrt{g_{m0} g_{m1}/(C_0 C_1)} \qquad Q = \sqrt{T \tau_0 \tau_1}/(\tau_0 + \tau_1) \quad (3)$$

The simulated frequency response for three types of CMF circuit [1]-[3] is shown in Fig. 2.

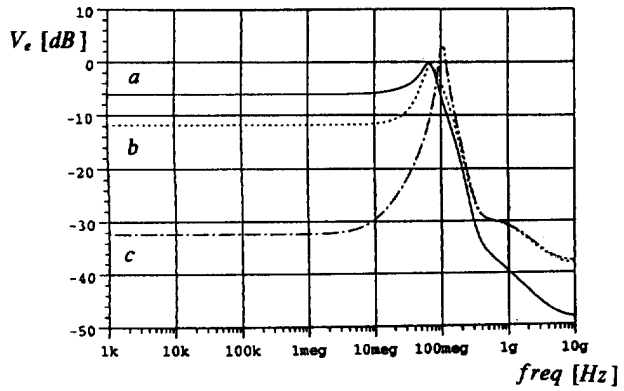

Fig. 2. The simulated frequency response of three basic CMF's: a) resistive degeneration of current mirrors [1] b) current injection [2], c) current steering [3].

It can be seen that all responses agree well with (2). In particular, the substantial peaking caused by two real zeros and two complex poles in the frequency response of V_e is visible, causing the CMF loop to lose its attenuation at higher frequencies. In extreme cases, peaking is so large that the CM gain of the loop becomes positive for certain frequencies and in case the phase shift is more than 180^o the CMF loop becomes unstable. Unfortunately, in most practical CMF circuits the peaking occurs in the operating range of a DMO AISP system, i.e., in the range of $10 - 200\,MHz$. Thereby, at high-frequencies a CMF loop loses its attenuation for the CM signals while still generating noise and distortion. From (3) it follows that Q of the pair of complex poles in the denominator of (2) is proportional to $\sqrt{T}$: the more dc "stabilization" is required from a CMF loop the higher a Q results.

On the other hand, it can be seen from (3) that increasing C_0, C_1 or decreasing R_0, R_1 results in lowering Q, which indicates a natural way of stabilizing a CMF loop. In such a case, the loop loses its attenuation even earlier due to the zeros moving to lower frequencies. Since the g_m-values of the CM-detector and the load current source have in practice additional phase shift due to their higher-order poles, this contribution can be modeled by $g_m(s) \approx g_{m0}(1 - s/p)$. The additional phase shift introduced into the CMF loop causes the enhanced Q to be $Q^* \approx Q/[1 - 2Q\,(\omega_o/p)]$ which can be derived from (3) assuming for simplicity that $g_{m0}/C_0 \approx g_{m1}/C_1$. From Q^* it follows that, e.g., for phase shifts as small as $0.1\,rad \approx 6^o$, with $Q = 5$ corresponding to T in the range of $30 - 40\,dB$, the CMF loop may become unstable. From the above analysis it can be seen that CMF circuitry can be very detrimental to the AISP system performance. Therefore, a preferred solution is to avoid the use of CMF circuitry entirely.

III. DEFINING DC OUTPUT VOLTAGE WITH $1/G_M$

A simple method of avoiding a CMF circuit is to load the output of a G_M-cell with a resistor. Thereby, the dc output voltage is defined and there is no need for CMF circuitry. Such an approach was adopted in [7] and [8] where a negative-impedance converter (NIC) was used to increase the output impedance. The penalty for using an NIC is additional distortion and noise. The NIC approach may also have problems with stability. It would be more convenient to be able to accept a finite positive resistance at the integration node and avoid the use of an NIC. However, if the filter is to be tunable a fixed resistor R at the output of a G_M-stage results in serious errors in the realized transfer function. As will be shown in Section IV, a convenient approach to synthesize a filter is to load a G_M-stage with a tunable resistor of value $1/g_m$. Consider the single-input single-output resistor $1/G_M$-stage in Fig. 3a [9]. If the input is connected to the output, I_B can be approximated as

$$I_B = C_{ox} \mu_n (W/L)_1 (V_O - V_{Tn} - 0.5\,V_{DS1})\,V_{DS1} \quad (4)$$

From (4) it follows that in order to maintain a constant dc output voltage V_O while tuning a filter by changing g_{m1}, i.e., V_{DS1}, the bias current I_B has to be adjusted. Note that

V_{DS1} is forced to be close to V_{TUNE} by the voltage amplifier A_{V1} in Fig. 3b.

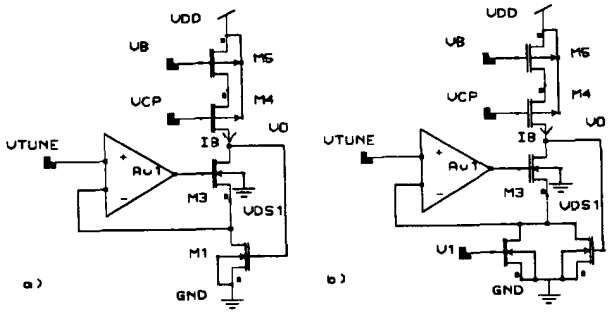

Fig. 3. The triode transconductor G_M
a) single-input single-output $1/G_M$ resistor
b) double-input single-output G_M loaded with $1/g_m$ resistor.

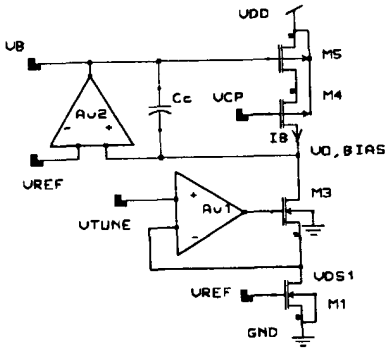

Fig. 4. The biasing scheme using a replica of the G_M–stage.

A suitable scheme for generating an adjustable bias current I_B is presented in Fig. 4. It repeats the G_M circuitry in Fig. 3 with an additional CMOS OTA A_{V2} acting as a simple differential voltage amplifier. A_{V2} compares the reference voltage V_{REF} with the output voltage $V_{O,BIAS}$ of the bias G_M and adjusts V_B so that $V_{O,BIAS} \approx V_{REF}$. The input of the bias G_M is also connected to V_{REF}. The bias voltage V_B is applied to all G_M-cells in the filter. Since the bias G_M is a replica of a G_M, from (4) follows

$$I_B \approx C_{ox}\mu_n (W/L)_1 (V_{REF} - V_{Tn} - 0.5\, V_{TUNE})\, V_{TUNE} \quad (5)$$

Substituting (4) in (5) it follows $V_O \approx V_{REF}$. Stability of the biasing scheme in Fig. 4 is secured by a small capacitor C_C. It should be noted that if matching between the bias G_M and the other G_M-cells were ideal the bias system would maintain a correct *dc* output voltage at the output of each G_M-cell even if $1/g_m$ resistors were not present. Practically, $1/g_m$ resistors are necessary to secure a proper bias point for non-ideal matching between the two G_M's.

IV. FILTER SYNTHESIS BY LOSSY INTEGRATORS

Building a cascade-design filter requires second-order sections (biquads). Additionally, if CMF circuitry is to be avoided both internal nodes of a biquad (LP and BP in Fig. 5) have to be resistively loaded. The resulting circuit presented in Fig. 5 built using lossy g_m–C–$1/g_m$ integrators, will be called "lossy biquad".

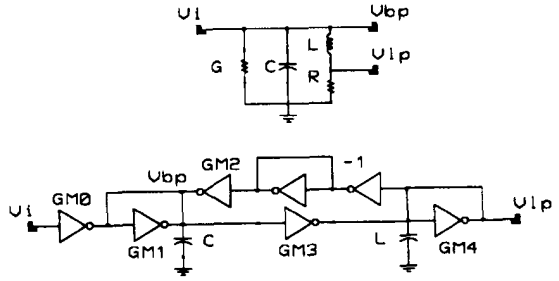

Fig. 5. The single-in single-out "lossy biquad":
a) RLC circuit
b) $G_M - C$ active simulation.

It realizes lowpass and lossy bandpass transfer functions given by

$$\frac{V_{lp}}{V_i} = \frac{g_{m0}g_{m3}}{D(s)} \qquad \frac{V_{bp}}{V_i} = \frac{-g_{m0}(g_{m4} + sL)}{D(s)} \quad (6)$$

$$D(s) = g_{mk}^2 + s(g_{m1}L + g_{m4}C) + s^2LC \quad (7)$$

where $g_{mk}^2 = g_{m1}g_{m4} + g_{m2}g_{m3}$. Note that both L and C are capacitors. From (6) the reason for loading the integrators with $1/g_{m1}$ and $1/g_{m4}$ rather than simply using resistors R_1 and R_4 becomes clear: if ω_o is wrong, g_{m1} to g_{m4} need to be readjusted. This might not be possible with fixed R's because they would not track the other g_m's. Using (7) the pole frequency ω_o and Q are given by

$$\omega_o = g_{mk}/\sqrt{LC} \qquad Q = g_{mk}\sqrt{LC}/(g_{m1}L + g_{m4}C) \quad (8)$$

If all g_m's are equal the highest achievable Q is $\sqrt{2}/2$ provided that $L = C$. In order to obtain an arbitrary Q assume that $g_{m1} = g_{m4}$, $g_{m2} = g_{m3} = g_m$ and $g_m = ng_{m1}$. In such a case it can be seen from (8) that $Q = 0.5\sqrt{n^2+1}$ with $L = C$. Note that if $|V_{lp}/V_i|$ of a "lossy biquad" needs to equal unity the value of g_{m0} should be adjusted appropriately. In a practical active realization additional losses due to loading the integrating capacitors L, C by the finite output impedances of the G_M–stages should also be compensated for. In order to simplify the circuitry of a "lossy biquad" a double-input G_M such as one in Fig. 3b is used. Rather than repeating the whole G_M–stage a single input device is added. Comparing the active simulations of Fig. 5b and Fig. 6 (top half) it can be seen that implementation using double-input G_M's results in nearly halving the circuitry. Using the approach described, single-ended cascade lowpass filters have been designed [10]. Other filter structures using lossy integrators are being investigated. The final goal of designing differen-

tial structures is achieved readily by using two single-ended filters in parallel and driving them differentially as in Fig. 6.

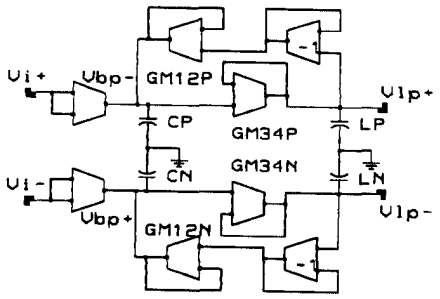

Fig. 6. The differential "lossy biquad" built with double-input G_M's.

Note that because of the nature of V-I conversion the single-ended G_M in Fig. 3b is linear; so is any single-ended filter built with such G_M–cells. The differential structures further improve the linearity by cancelling all even harmonics as well as power supply or CM noise.

IV. CONCLUSIONS

A method of avoiding CMF circuitry in continuous-time g_m–C filters has been proposed. The drawbacks of CMF circuitry, including poor high-frequency performance, problems with stability, as well as associated additional power, die area, distortion and noise, have been pointed out. The *dc* output voltages in the method presented are defined by use of lossy integrators in connection with a precise biasing scheme. The accuracy of setting the *dc* output voltage for 10:1 tuning range of g_m is demonstrated in Table 1.

Table 1. Output dc Voltage Variation for $V_{DD} = 5\ V$

V_{TUNE}	I_B	g_m	V_{BP}	V_{LP}
1250 *mV*	145 *uA*	51 *uS*	2475 *mV*	2513*mV*
1500 *mV*	704 *uA*	270 *uS*	2498 *mV*	2500*mV*
1750 *mV*	1159 *uA*	496 *uS*	2501 *mV*	2497*mV*

An active g_m–C filter synthesis method using lossy g_M–C–$1/g_m$ integrators has been demonstrated. The expected advantages of this approach for the design of integrated fully-differential continuous-time filters include simpler circuitry due to elimination of all CMF circuits, improved stability, reduced power, die area, distortion and noise. The described approach is naturally suited to lowpass cascade filters but other filter structures are being also investigated.

ACKNOWLEDGMENT

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