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ON AUTOMATION PLACEMENT AND ROUTING OF GATE ARRAY

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S u m m a r y

The paper presents the idea and the recent results of the application of the system of designing a two-layer metalization mask in bipolar logic matrices. Two basic parts of the designing system are presented: the algorythm placing the cells and the algorythm routing the interconnections.

The description of algorythms is illustrated with drawings. A drawing of the matrix is presented in which the metalization has been generated automatically by means of the above system.

1. Introduction

The paper presents a CAD method of bipolar Gate Array design. The array consists of regularly placed, quasi-square cells with horizontal and vertical channel for interconnections. Two layers for connections are permitted /Fig. 1/.

The layout design procedure has two steps:

1/ simultaneous placement and initial tracing of connections,

2/ final routing, defining the geometry of connections and partitioning of two metalization layers.

The placement is based on building up the array "cell by cell". For consecutive step the sets of unplaced cells and available places in the array are searched. Unoccupied cells situated in the neighbourhoods of the cells which have already been placed, make the set of available places. Search is

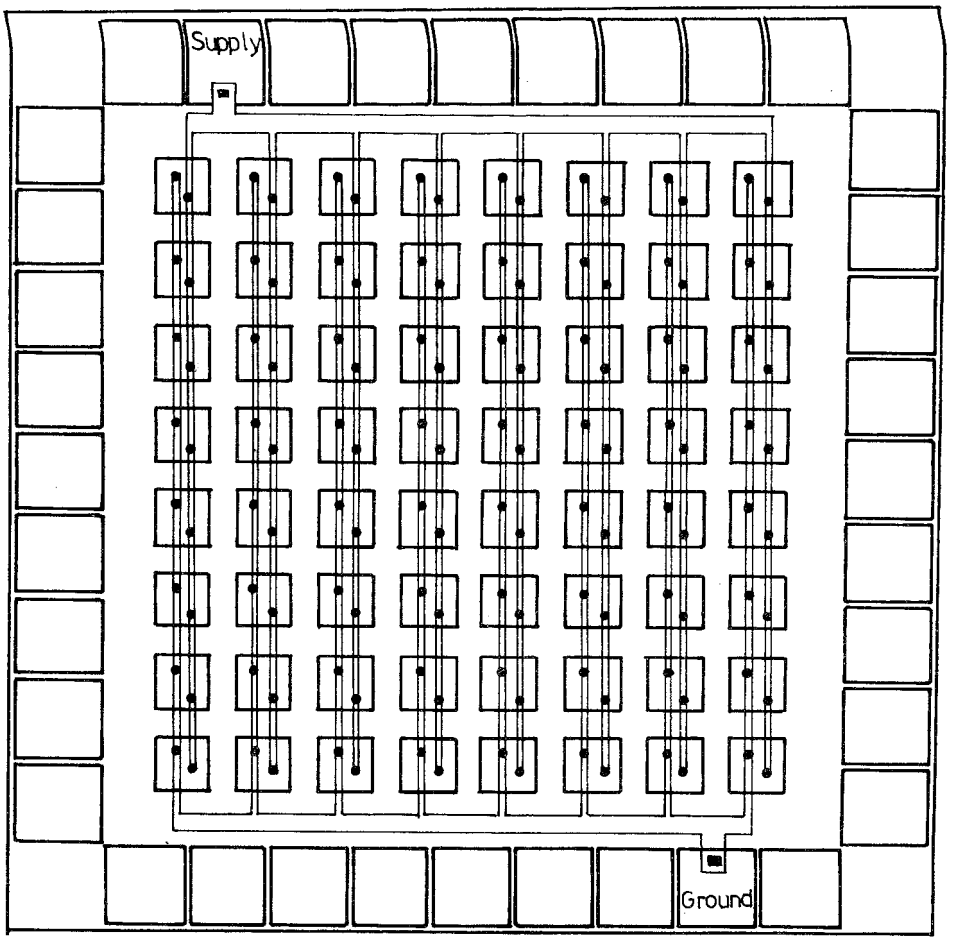

Fig. 1. The layout of Gate Array with: - 64 cells, - 36 bonding pads, - supply and ground tracks. Regularly placed cells form vertical and horizontal channels for interconnections

made for cells which have the greatest number of contacts not yet connected. A cell and a place are chosen basing on the minimum value of the target-function. The processed cell is permanently fixed in the chosen place of the array. Simultaneously, the tracks of connections to the placed cells are made. These tracks will form the data base for the final routing step.

The final routing starts when all cells have been placed. Connections paths of each channel of array are projected

separately. Channels can be projected in any order. First a sequence of tracks in the chosen channel is analysed. Sequence is defined as transversal order of tracks, from one edge of the channel to the other. Then the sequence is chosen which minimises the number of parasitic couplings between signal paths and the number of layer changes. With such sequence, the exact connection paths, based on geometry rules, are established.

If connections path goes through more than one channel, the path is projected partially. Only this fragment of the path is designed, which is included in the considered channel. The process of designing is repeated for each channel of array in sequence.

As the result, coordinates of each segment of metalization with specified number of layer are obtained.

2. The metod of automatic placement and tracing the connections

2.1. Principles

The construction of placing and tracing algorithms is based on the following principles:

- the array dimensions are known and the total number of cells is greater than the number of cells for placing,
- the cells are square or rectangular with sides length ratio close to 1,
- the cells orientation is fixed,
- single cell or rectangular block of cells can be placed,
- the bonding pads are regularly placed on 4 array sides,
- the channel widht is given,
- the connections are led in two metalization layers,
- the connections are led in channels only, the areas of cells or blocks of cells are forbiden for external connections,
- the ground and supply tracks are hand-designed and their shapes are not changed in the routing step.

2.2. Placing with simultaneous tracing the connections algorithm

The algorithm yields the placing which is close to the optimum one. It is not optimum as the result of a limited number of checkings. In spite of this limitation, the placement still maintains adequate quality.

The algorithm belongs to the group of constructive algorithms, the final result is obtained by adding successive cells to the group of cells alresady placed /Fig. 2/.

Target-function is determined by the criteria of choosing a cell for placing. This function is based on the connection length between cell to be placed and those already located. The location of new cell is found as follows.

The set of placed cells with unrouted connections is created and searched. The neighbourhood of the cells with many unrouted connections is searched first since it is there where the highest probability of finding appropiate place for cell location exists /Fig. 3/.

The placing graph construction is shown in Fig. 4.

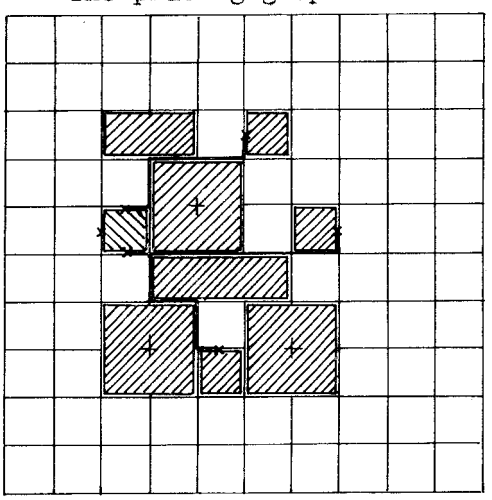

Fig. 2. The placing of a single cell with tracing the connections to the cells or blocks of cells which have already been placed

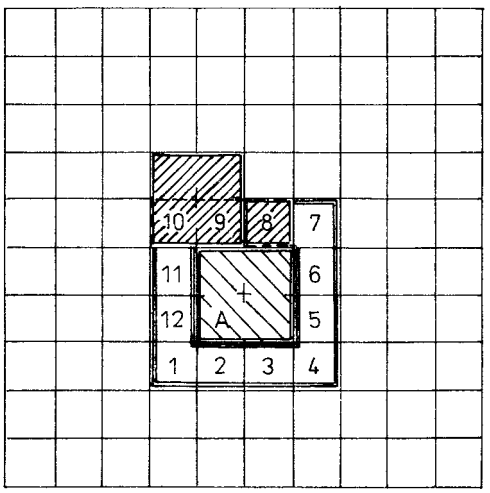

Fig. 3. The neighbourhood of block of cells A. The cells with numbers 8, 9, 10 are occupied

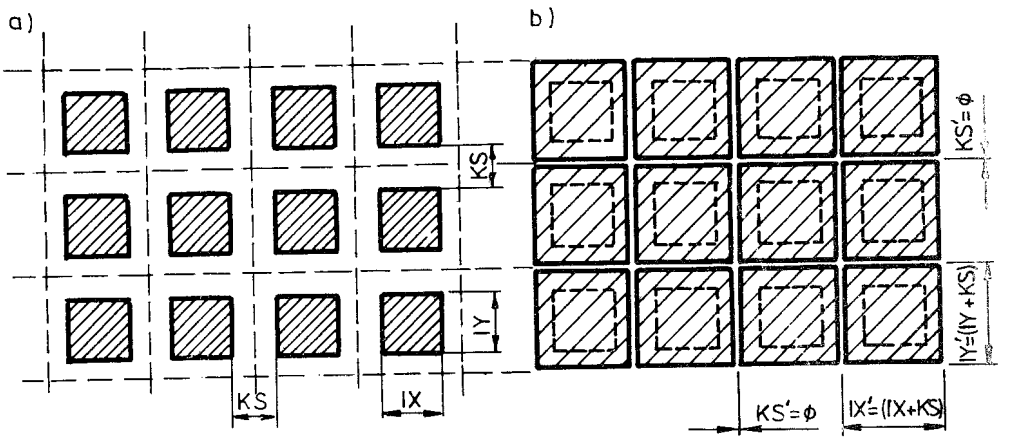

Fig. 4. The placing graph construction: a) placing the cells of dimensions IX × IY separated by the channels of width KS, b) placing the cells of dimensions (IX+KS) × (IY+KS) separated by the channels of zero width

2.3. Time relations of the placing algorithm

Let us assume that n identical cell are to be placed and each locating requires the same number of operations. Each cell has the neighbourhood consisting of 8 cells. After introducing an assumption which allows to place in the neighbourhood of a given cell, only the cells being connected with this one, the number of operations N, for the k-th placement step would be described by following inequality:

$$N(k) \leqslant 8 \cdot l \ ,$$

where l is the number of cell's connections.
The total number of operations is the sum:

$$N_t = \sum_{k=1}^{n} N(k) = \sum_{k=1}^{n} 8 \cdot l = 8n \cdot l \ ,$$

finally

$$\boxed{N_t \sim n}$$

Thus, complication function of the algorithm becomes linear dependence on the number of the cells.

2.4. The final routing algorithm

The purpose of this part of designing is to establish precise paths of metalization. Only the network of connections between cells and blocks of cells is to be designed. The connections inside cells and blocks are given in advance.

The correctly designed connections must fulfil the following requirements:

1/ connection resistance ought to be as low as possible. This is achieved by minimizing the total connection lenght and the number of vias /metalization layer changes/.

2/ parasitic coupling between signal paths ought to be as low as possible. This is achieved by minimizing the number of path crossings and by increasing distances between the paths.

3/ the obtained connection paths must not decrease production yield. This depends fully on the first two demands and the minimum number of the path turnings.

It is very difficult to obtain a solution with the best electrical parameters of I.C. and with the highest production yield. The main problems to overcome are; defining precise algorithm target-function /many significant factors/ and time computing limitation. Actually however, a "feasible" rather than the optimum solution is searched.

It is possible to resolve this problem by symplifying target-function so that only the most powerful parameters are taken. Such into account simplified algorithm gives nonoptimal results but by selecting proper target-function acceptable results can be obtained.

To simplify the problem it has been assumed that:

1/ only vertical and horizontal path segments are permitted. The connections length increase caused by this assumption will be small due to specific gate array shape.

2/ the paths going transversly to the supply and ground lines are placed on the first metalization layer, the paths going along them are placed on the second layer. The supply

and ground tracks are by definition placed on the second layer, the paths crossing them must run on the opposite layer.

3/ path placement in the channel are quantified with module equal to the minimum distance between two parallel paths /technological restriction/. The path locations are allowed in strictly defined places called lines /Fig. 5/. Connection paths in logical circuits have usually constant width, so this limitation has little influence on the design results.

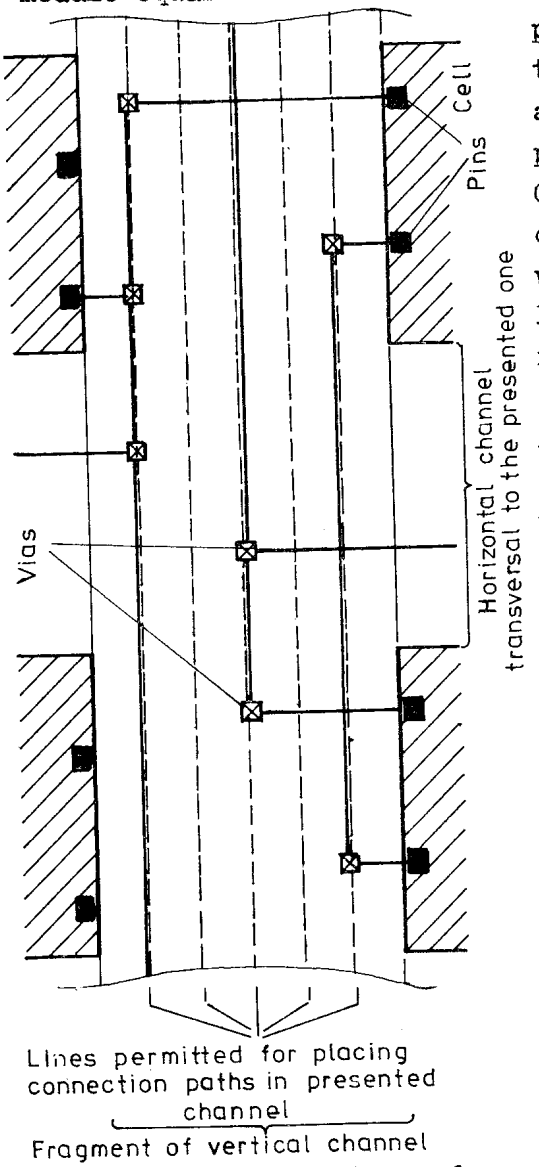

Fig. 5. Magnification of a channel fragment. Broken lines mark the axes of connection paths

4/ each channel of gate array is designed separately. This is the most powerful simplification as it influences the path-intersection number, but it allows considerably less complicated algorithm to be used and speeds up the procedure.

With the above assumptions, the metalization design reduces to assigning connection paths segments to the earlier defined lines in the channel /as the result of the 3rd principle/.

Metalization path length is determinated by the distance between the chosen line and the connection pins /Fig. 6/. The number of path crossings is determinated by the sequence of chosen line in relation to other path lines /Fig. 7/.

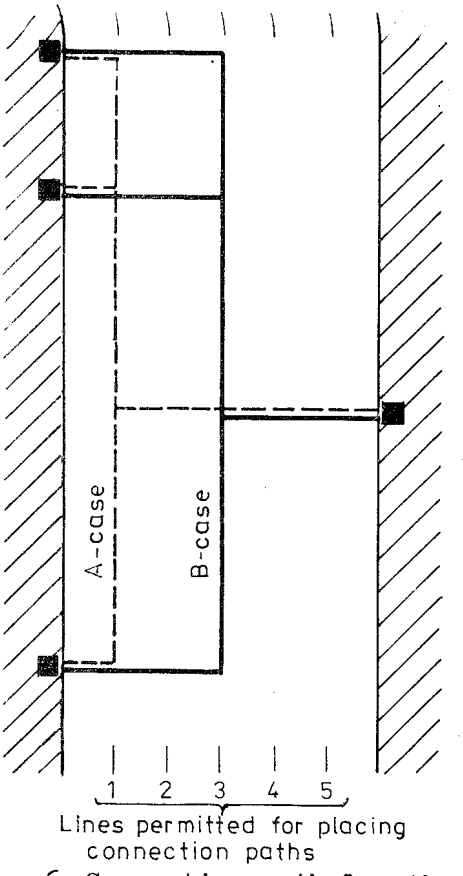

Fig. 6. Connection path length is determined by the distance between the chosen line and the connection pins. In A-case /chosen line No 1/ the total length is lower than in B-case /chosen line No 3/

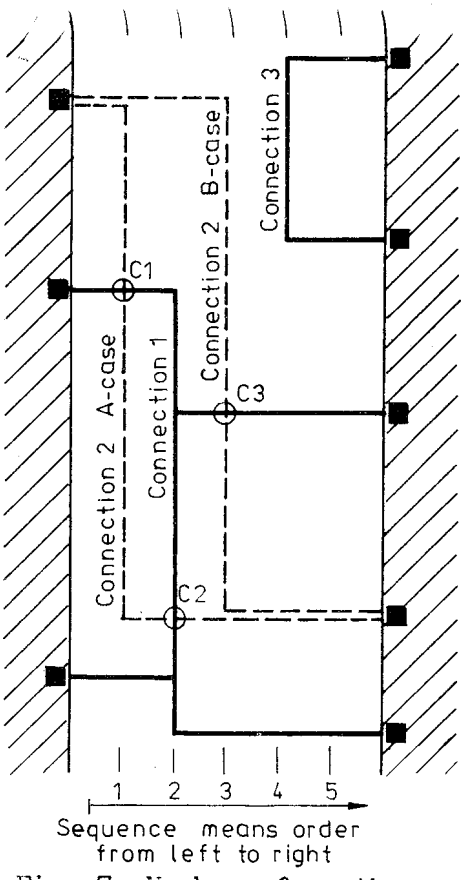

Fig. 7. Number of path crossing is determined by sequence of chosen line in relation to other path lines. For connection No 1 there are two orders /from left to right/: A-case, sequence 2-1, crossings C1 and C2, B-case, sequence 1-2, crossing C3

It should be pointed out that, the channels in which connection paths go are determinated by the placing algorithm. The final routing algorithm has no possibility to change them, it only generates proper path shapes. The routing algorithm has little impact on path length but major one on intersecting of paths. So the primary goal of tracing is to determine the optimum connection paths sequence in channels, which minimize the number of path crossings.

This sequence is established at first for a given channel. In the next step, rectilinear path segments are placed on channel lines preserving the previous sequence. If path segment could be located on one of several lines the line which provides the shortest path length is chosen.

3. Final results

The system based on the principles of the presented method is called MATRIX. It has been programmed in FORTRAN IV and implemented on ODRA 1305 /ICL 1900/ computer under GEORGE-3 control. The system is fully automatic. The user can interact only between the programs. If not satisfied he can modify some parameters for the next step. There is no graphical interaction.

The final results of the system action are as follows:

- the array drawing with an exact design of metalization paths /Fig. 8/,
- the data file describing the metal mask of array; this file is used for Pattern Generator control.

The system consists of 5 programs and occupies the memory of maximum 48 K of 24 bit words.

The "placement" part of the system consists of 2 programs:

1/ reading, testing, and preliminary processing of entry data,

2/ placing the cells with tracing the connections and creating the data used in metalizations design program.

The "metalization design" part of system has 3 programs:

1/ reading, testing and preliminary processing of entry data,

2/ routing design in all array channels,

3/ creating the data files for plotter and Pattern Generator.

Basing on the results of each program, the user can trace the process of designing and modify some parameters in the program if necessary. In particular, the user has a possibility

of placement appreciation between the first and the second part of the system. The symbolic drawing of gate array allows one to see the cell location process.

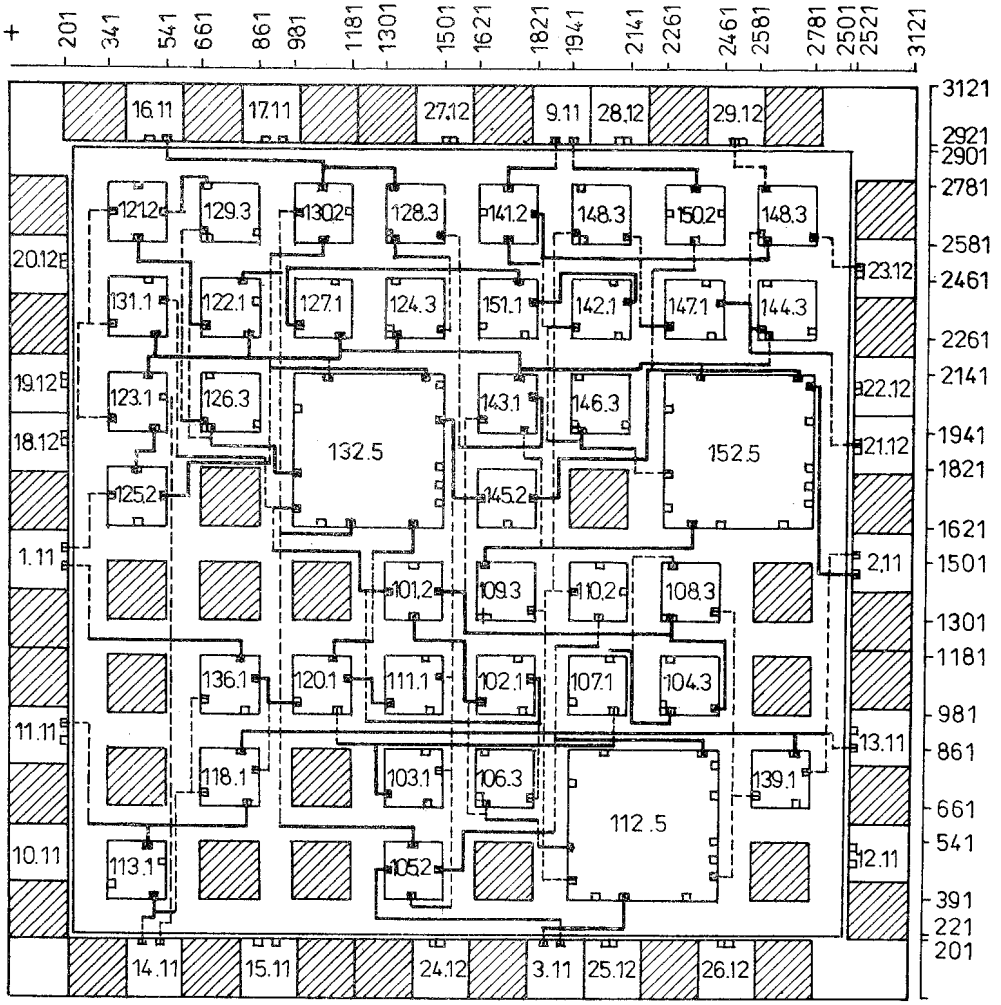

Fig. 8. The test Gate Array layout drawing from plotter

The processing time is proportional to the number of the cells, for placing algorithm. The results are presented in Tab. 1.

Table 1. Placement program results

No	1	2	3
Number of cells	4	21	120
Number of nets	12	26	84
CPU time in mins	1.1	3.2	20.6

The user has possibility of semi-interaction in routing program too. If metalization paths are not satisfactory for him, the project of each channel can be repeated with changed parameters. The run time of routing is nearly linearly dependent on the number of rectilinear path segments. The results for 3 programes are presented in Tab. 2.

Table 2. Routing program results

No		1	2	3	4
Number of cells		4	40	40	120
Number of nets		12	15	35	84
Number of path segments		30	110	190	402
CPU time in mins	1st program	2.1	6.5	14.1	35.5
	2nd program	2.5	7.5	16.	29.8
	3rd program	3.	6.1	7.1	16.3
	total time	7.6	20.1	37.2	81.6

The actual version of MATRIX system could design gate array up to 625 cells /25x 25/ with 64 bonding pads.

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