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I/O-PADS PLACEMENT ALGORITHMS

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A b s t r a c t

Two basic I/O-pads placement algorithms are presented. The first of them is convenient in the case of a given I/O-pads sequence, the second one designes this sequence. Besides, there are further versions of these two basic algorithms including the possibility of I/O-pads grouping and the existence of connections between I/O-pads. The algorithms were implemented in an automatic metal mask designing system for Gate Arrays.

1. Introduction

The modern ICs: VLSI and especially Gate Arrays are equipped with many inputs/outputs. Often, there is a need to design an IC having more then 100 or even more then 200 inputs/outputs.

Input/output blocks often perform logical functions and have a few connection pins each, to the circuit's inner blocks. Sometimes, I/O blocks are connected together by signal paths. Such a large amount of I/O-pads in an IC results in facing the optimum placement problems. The connections from I/O-pads to the circuit interior should be as short as it is possible, which is not always easy to satisfy. Non-optimum I/O-pads placement can cause the connections to be long. Moreover, hand-designed multiple I/O-pads placement costs a lot of designer's time and can introduce errors into the project. For all these reasons,

for the purpose of automatization and optimization of the design process, some I/O-pads placement algorithms, meeting various design requirements, have been developed.

2. I/O-pads placement strategies

For an IC layout design two situations are typical:

- I/O-pads sequence is given by a customer, or an IC is pin to pin compatible to another IC.
- I/O-pads sequence is to be designed.

In the first case, as the pads sequence is given the I/O-pads placing is obvious. Having the first pad placed according to the make-up rules the next pads are regularly placed in the proper direction and order. It is important that inner blocks are placed after the I/O-pads /Fig. 1/. Such a sequence allows the length of connections between the inner blocks and I/O-pads to be minimized, during the placement of the inner blocks. As a result these connections tend to be of the quasi-optimum length, which is equivalent to the situation when I/O-pads placement is designed to obtain the similar effect. In the case of placing the inner blocks, an algorithm is used which takes into account connections to I/O-pads and minimize their length /e.g. [1] or [2] /. This results in a quasi-optimum layout, in spite of a fact that I/O-pads placement has been given.

In the second case, when I/O-pads sequence is to be designed, the oposite sequence of design steps is chosen: at first inner blocks and then I/O-pads are placed /Fig. 2/. When I/O-pads are placed, the length of the connections to the inner blocks in minimized. The resulting connections become of a quasi-optimum lenght, and the whole layout becomes a quasi-optimum one.

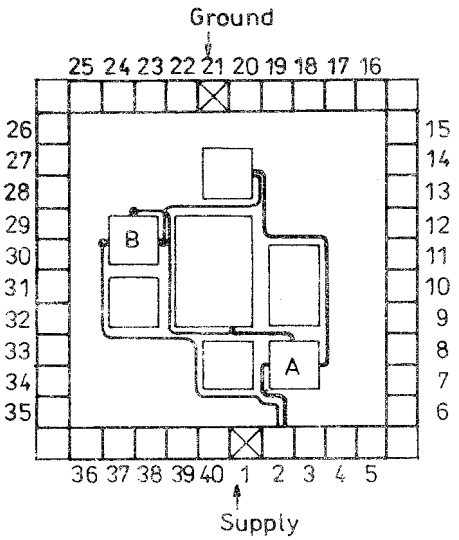

Fig. 1. The idea of inner blocks placing, taking into consideration a given I/O--pads placement. For the given block two placing positions are considered-"A" and "B". "A" position is chosen having shorter connections

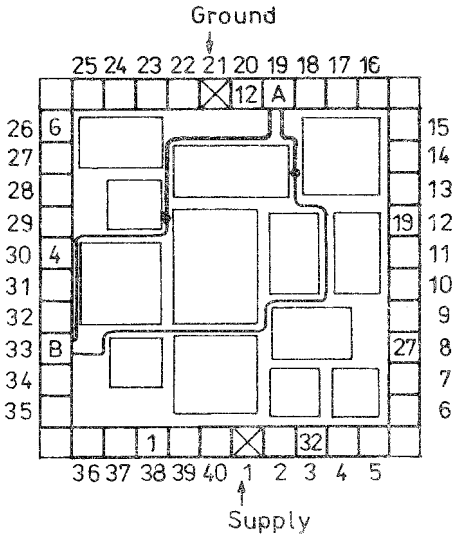

Fig. 2. The idea of I/O-pads placing, taking into consideration a given placement of the inner blocks and already existing interconnections /unvisible in the picture/. From two positions of a pad-"A" and "B", "A" is chosen having shorter connections

3. Placing of I/O-pads groups

Ammong I/O-pads to be placed there are often ensembles consisting of many inputs or outputs. These sets are called I/O-pads groups /Fig. 3, 4/.

An I/O-pads group is defined as a set of I/O-pads, in which all elements, except the two boundary ones, will always neighbour the same group's members.

The exception of this rule are supply and ground pads, which are not taken into consideration while defining the neighbours of the given I/O-pad /Fig. 3/.

The I/O-pads group's sequence is given. The introduction of a group term makes sense only in the case when the sequence of

the groups is to be designed. In the case when the whole I/O--pads sequence is given the introduction of additional I/O--pads subsets, in a form a groups is useless.

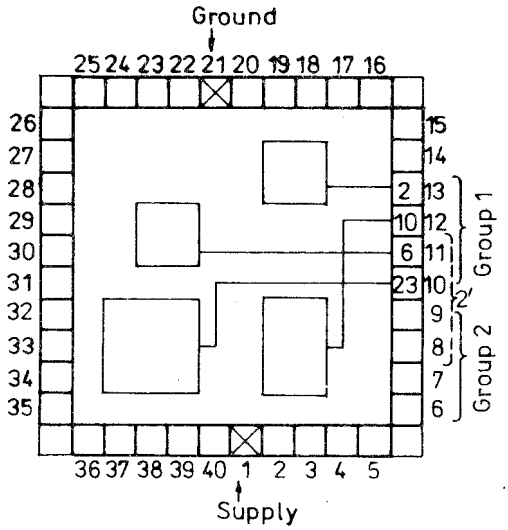

Fig. 3. Design of the placement of single I/O-pads and I/O-pads groups. At first the group 1 has been placed. The optimum location of the group 2 /dashed line/ overlaps the location of the group 1 /positions 12 and 13/. The possible locations of the group 2 are positions from 8 to 11. Positions 1 and 21 are reserved

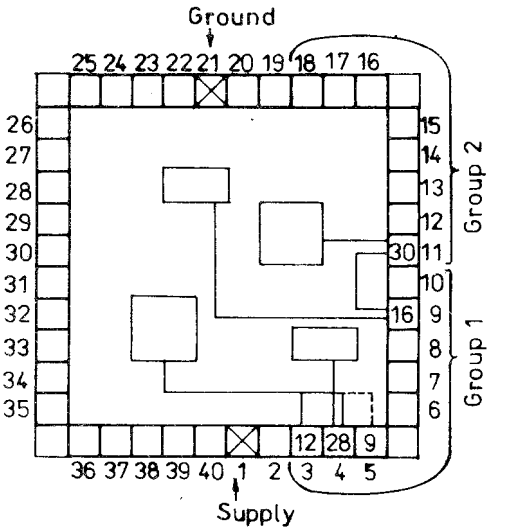

Fig. 4. Placing of single I/O--pads and I/O-pads groups while there are existing connections between I/O-pads. These connections can be led between the pads of the same group /pads 12 and 28/ or between the pads from different groups /pads 16 and 30/. Pad 9 can be connected /dashed line/ only after placing of pad 28

I/O-pads placement while I/O-pads groups exist, consists in building the list of optimum locations of groups or single pads. This list is produced by checking the total connection length to inner blocks of IC for each group /or single pad/ and for each available location of group /or single pad/. Next, the minimum with respect to all available locations is found and this value as well as its location are placed on to the list.

The list is sorted with respect to decreasing connection length. The first group for placing is chosen having the greatest optimum length. This group is permanently located on the optimum position and all connections to inner blocks are led. Next, the group is erased from the list. Then, successively the next greatest length of a connection group or a single pad is chosen. An attempt is made to place it on its optimum location. If it is not possible, as all optimum positions are occupated by earlier placed groups, a list of available locations for the given group is created. Then location from this list is chosen which results in the shortes connections length. The group /or single pad/ is parmanently located on the chosen, quasi-optimum place and all connections to inner block are led /Fig. 3/. The group is erased from the list, and the next group with maximum connection length is searched on the list. The procedure is repeated until the last group /or single pad/ is placed.

For such a procedure it is obvious that the first group and perhaps few others are gaining possibility to be located on the optimum positions. These groups /or single pads/ have the longest connections. Further groups /or single pads/ have shorter connections. Because of the lack of the place they can be placed on non-optimum positions. In spite of that, the increase of the connection length is supposed to be on the average, smaller than for the groups with the longest connections. Thus, a solution derived from above method is not an optimum but a quasi-optimum one.

4. Connection between I/O-pads

If such a connection exists, the placing algorithm ought to be modified. For this purpose, position of group /or single pad/ as well as the lenght of the connections to the inner blocks and to all already placed I/O-pads is to be found. Similary,

the connections after placing a group /or single pad/, are led to the inner blocks and to all already placed I/O-pads /Fig. 4/.

5. Summary

On the base of the above considerations a few versions of two basic I/O-pads placement algorithms have been constructed. These two basic algorithms are: placement of a given I/O-pads sequence and I/O-pads placement design. Individual versions differ from each other by applying the I/O-pads grouping or not, and by taking into consideration the connections between I/O-pads or not. Two programms containing all versions of the presented algorithms were developed. A user has an opportunity to chose the proper version. Both programs were written in FORTRAN IV. They are a part of a system "MATRIX" [2], which fully automaticly designs metal masks for Gate Arrays.

References

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2. W y s z y ń s k i A., K u b i a k R.: On automation placement and routing of Gate Array. ECCTD 85 Conference Proceedings. Prague, September 1985.