High-Frequency Linear Tunable Single-Ended

Voltage to Differential Current Converter

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ABSTRACT

A single-ended to differential (*S-D*) tunable voltage-to-current converter can replace a *S-D* voltage-to-voltage converter or a transformer. The resulting system is simpler and has better high-frequency performance. Measurements show that for a *9 GHz* bipolar process with a power supply of *0 - 5 V*, *THD* < *0.15%* for an input voltage of *1.2* V_{pp}, the signals are in anti-phase up to *120 MHz*, the tuning range of g_m is *150 - 750* μS, and the signal-to-noise ratio reaches *65 dB* for the bandwidth of *500 MHz*.

I. INTRODUCTION

Analog signals coming from an antenna or a sensor are naturally referred to the ground terminal. These signals when processed by single-ended circuits are further referred to one common terminal, whereas differential circuits use two signals in anti-phase referred one to another. Doubling the signal-level, reduced distortion due to cancellation of all even-order harmonics, and improved common-mode and power-supply rejections are among advantages of differential over single-ended analog signal processing. Although differential-mode of operation results in increased circuit complexity, and larger dissipated power and die area, these overheads are justified by substantially improved performance of analog front-ends. Since the input to the system is single-ended, but the rest of signal processing is preferably differential, there must be a block on the system converting a single-ended signal into a pair of differential signals. In case of equipment built with PCBs, the single-ended to differential (*S*-D) conversion may be performed with the use of transformers. Even miniature RF-transformers such as [1], have a half-inch feature size, and reveal bandpass transfer function with highpass roll-off at *10 ÷ 100 kHz* and lowpass at *100 ÷ 300 MHz*. Moreover, since transformers are built as discrete elements, additional band loss associated with board parasitics practically precludes their use above *50 MHz*. Additionally, due to the nonlinear characteristic of the magnetic core material transformers suffer from harmonic distortion and hysteresis. In the case where there is no physical space for a transformer, the operational frequency is high, the required distortion level is critical, or operating from *dc* to VHF is required a monolithic active *S-D* converter should be applied. Obviously, even if a transformer can be used the fully-monolithic solution is always cheaper and more reliable.

II. S-D V-I CONVERTER

Consider the model of a system in Fig. 1a, that consists of a pre-amp, a *S-D* voltage-to-voltage (*V-V*) converter, followed by an anti-aliasing (a-a) filter, and a mixed-mode analog and digital signal processing block (M-MSP). If the a-a filter is realized using g_m - *C* techniques

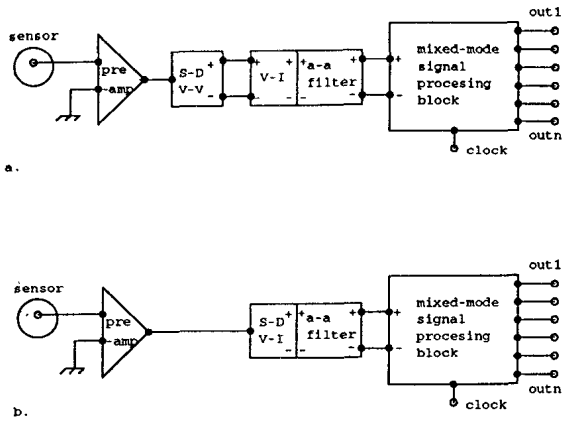

Fig. 1. Two possible approaches to realizing an analog front-end system:
a) a pre-amp, a *S-D V-V* converter, an a-a filter, and M-MSP.
b) a pre-amp, an a-a filter, and M-MSP. *S-D* conversion is performed inside the a-a filter by a *S-D V-I* converter.

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its first block is always a voltage-to-current (*V-I*) converter. Therefore, a possibility exists to combine the *S-D V-V* converter with *V-I* converter of the filter to form a *S-D V-I* converter and totally avoid the *S-D V-V* converter, as shown in Fig. 1b. This may result in improved high-frequency and noise characteristics of the whole system, as well as power and die area savings. The *S-D V-I* converter shown in Fig. 2a, is built as a tunable transconductor

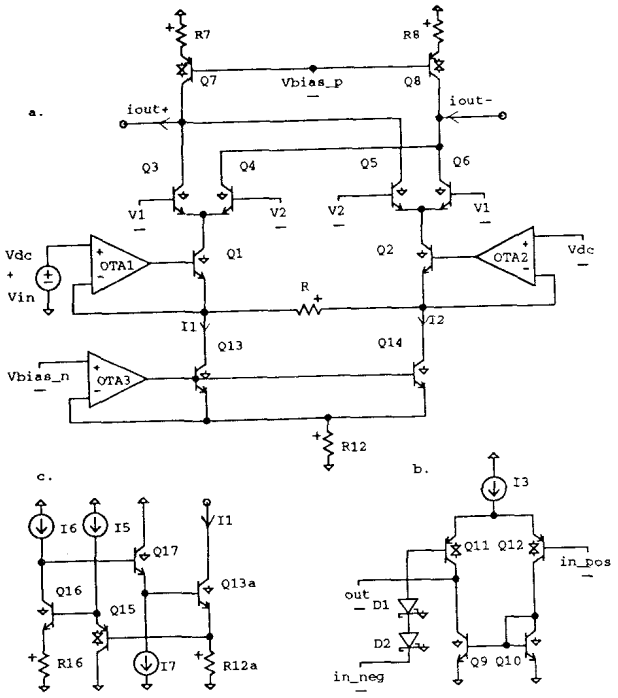

Fig. 2. Bipolar single-ended to differential tunable voltage-current converter: a) one-sided driven tunable G_M.
b) *pnp* OTA with a Schotky diode input level shift.
c) bipolar low voltage high output resistance current source.

denoted by G_M [2], [3]. The circuit is driven from one side only with its second input connected to a *dc* bias voltage. It is built with a pair of voltage buffers *OTA1*-Q_1, *OTA2*-Q_2 controlling the resistor R [4], [5]. For the purpose of g_m -tuning two cross-coupled pairs Q_3 -Q_4 and Q_5 -Q_6 are used [6]. Rather than using *T*-configuration consisting of one tail current source and two degeneration resistors, a *Π*-configuration formed by pair of current sources I_1 and I_2 driving one resistor is used. The latter results in a wider input linear range since in quiescent state there is no *dc*-drop across the resistor, neither does it suffer from g_m -mismatch due to *1 %* resistor tolerance as in case of *T*. Note that to reduce the output *dc*- voltage offset due to the mismatch between I_1 and I_2, the degeneration resistors of both current sources are combined in R_{12} as shown in Fig. 2. From [4] it follows that with enough voltage drop $2I_1R_{12} >> V_T$, the few percent mismatch error in saturation currents is reduced $(1 + 2g_mR_{12})$ - times, while matching of α's remains as good as a fraction of percent. The gain a_{v1} of *OTA1* forces a highly-linear *V-I* conversion by increasing the effective g_m of Q_1 a_{v1} -times and reducing the associated nonlinearity by the same order. The transconductance of the driven side can be approximated as

$$g_m^+ = \frac{\partial i_{out}^+}{\partial v_I} \approx \left(\frac{1}{R_{o1}} + \frac{\alpha_1}{2R} \frac{1}{1 + \frac{1}{a_{v1}\, g_{m1}\, 2R}} \right) f_1 \qquad (1)$$

where R_{o1} is the output resistance of the source I_1, α_1 is the nonlinear current gain of Q_1 , and f_1 is the g_m - tuning function of cross-coupled pairs Q_3 - Q_4 and Q_5 - Q_6, defined as

$$f_1 \approx \alpha_3 \, th\left(\frac{V_1 - V_2}{2V_T} \right) \qquad (2)$$

Note that with the output of I_1 swinging widely an additional *ac*-current is flowing through Q_1 . For the grounded side, *OTA2* forces the voltage variation at the emitter of Q_2 to be closely at *ac*-ground so the transconductance of this side is practically independent of R_{o2} as

$$g_m^- = \frac{\partial i_{out}^-}{\partial v_I} \approx \frac{\alpha_3}{2R} \frac{1}{1 + \frac{1}{a_{v1}\, g_{m1}\, 2R}} f_2 \qquad (3)$$

where $f_1 \approx f_2$ provided $\alpha_4 \approx \alpha_5$ and $\alpha_3 \approx \alpha_6$. Note also that cross-coupling substantially reduces α-errors.

For the optimum output swing, the resistance $R_{o,p}$ of the *pnp*-load sources Q_7 -R_7 , Q_8 -R_8 should be only slightly higher than that of $R_{o,n}$, made of a parallel connection of $R_{o3} \,||\, R_{o5}$, each of them being somewhat limited by the low resistances $1/g_{m4}$ and $1/g_{m6}$ acting as the effective degeneration resistors for Q_3 and Q_5 . $R_{o,n}$ can be expressed as

$$R_{o,n} = \frac{V_A}{I_1}\left(1 + \frac{1}{2m} + \frac{m}{2}\right)$$
$$m = e^{\frac{V1 - V2}{VT}} \qquad (4)$$

where V_A is an Early voltage. From (4) it follows that $R_{o,n\,max} = 2V_A / I_1$ for $V_1 = V_2$, and it is always less

with $V_1 \neq V_2$. For this design $50\ k\ \Omega < R_{o,n} < 250\ k\Omega$ and $R_{o,p} \approx r_{o7}\ (1 + r_{\pi 7} \parallel R_7) \approx 235\ k\Omega$ *OTA1* in Fig. 2b [2] is built as a *pnp* differential pair with a Schotky diode level shift at the input. Its gain is limited by the loading effect of Q_1 which reduces the output resistance to $r_{\pi 1}$. Hence $a_{v1} \approx r_{\pi 1} g_{m7} = \beta g_{m91} / g_{m7} = \beta_1 I_1 / I_3$. The input and output swings of S-D converter are $+- 0.75\ V$, but they could be extended to maximum of $+-1.0\ V$.

III. REDUCTION OF g_m- ERROR

The absolute g_m-error defined as $|\Delta g_m| = ||g_m^+| - |g_m^-|| \approx \alpha_1 / R_{o1} \approx \alpha_1 / r_o\ (1 + g_m R_{12})$ should be ideally zero. For the design $I_1 = 800\ \mu A$, $V_A = 20\ V$, $R = 1125\ \Omega$, and $R_{12} = 125\ \Omega$, would give $R_{o1} \approx 120\ k\Omega$, and the relative-error $|\Delta g_m / g_m| \approx R / R_{o1} \approx 0.93\ \%$. A good approach to lower this error without sacrificing the output swing is to boost R_{o1} with an active enhancement scheme [7]. One possible variation of this technique [3], shown in Fig. 2c, is used to obtain a high-resistance bipolar low-voltage current source. The top of the degeneration resistor R_{12a} drives through the *pnp* level-shift, Q_{15} - I_5, a gain stage, Q_{16} - R_{16} - I_6. The minimum required headroom for this source is $V_{CE13a,on} + V_{R12a} < 600\ mV$. To prevent the loss of gain due to loading of $r_{\pi 13a}$, the gain stage is buffered by *npn* follower, Q_{17} - I_7. With $\beta_1 \approx 100$, the output resistance is boosted to $R_{o1}^* \approx \beta_1\ r_{o1} \approx 2.7\ M\Omega$, and the error is reduced to $|\Delta g_m / g_m| \approx 0.04\ \%$. Note that the gain of stage Q_{16} - R_{16} - I_6 should be at least *100*. As a comparison a regular cascode achieves less than a half of R_{o1}^* and requires *0.9 V* more of headroom, while an improved cascode source using a smart biasing of the cascode transistor can have similar R_{o1}^*, but its swing is reduced by *0.5 V*.

IV. RESULTS OF MEASUREMENTS

The circuit was fabricated using *9 GHz* complementary bipolar process. The key design parameters of the available devices are given in Table 1. For the purpose of

Table 1. Device Parameters

Parameter	*npn*	*pnp*
$\beta_{F,peak}$	95 - 165	20 - 36
LV_{ceo}	*≥8V*	*≥8.5V*
V_A	*15 - 23 V*	*8 - 15 V*
f_T	*9.3 V*	*5.5 V*

dc-measurements both sides of the circuit were resistively loaded with on-chip *2.5 kΩ* loads. The measured *dc*-transfer curves of the converter are presented in Fig. 3. The linear range is *1.5* V_{pp} for a power supply of *5 V*. The measured performance of the converter in Fig. 2 is summarized in Table 2, where "s-s out." stands for "single-sided output-referred", and *500 MHz* bandwidth (BW) was taken rather conservatively, since for many applications filter's roll-off, usually located below *100 MHz*, practically defines the BW.

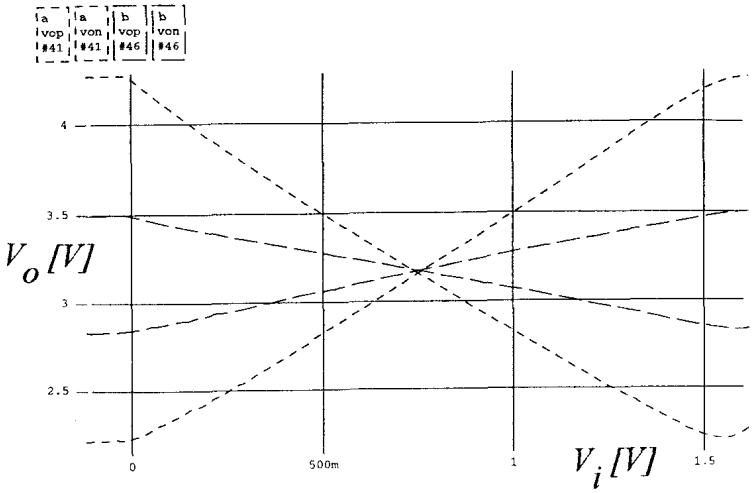

Fig. 3. Measured *dc*-transfer of the converter loaded by *2.5 kΩ* resistors for different g_m - tuning voltage V_2 - V_1: a) $g_m = 560\ \mu S$, b) $g_m = 160\ \mu S$.

Table 2. Measured Performance

Parameter	Measurement	Comment
power supply	*0 - 5 V*	*0 - 3.3 V pos.*
max. input	*1. 5* V_{pp}	*2. 0* V_{pp} *pos.*
g_m range	*150 - 750 μS*	*best perform.*
$\|\Delta g_m/g_m^+\|$	*0.1 %*	*typical*
s-s out. noise	*410* μV_{RMS}	*BW 500 MHz*
dif. out. noise	*580* μV_{RMS}	"
s-s S/N ratio	*60.3 dB*	V_i *= 1.2* V_{pp}
dif. S/N ratio	*64.6 dB*	"
dissip. power	*12 mW*	without load

As a comparison a wideband transformer [1] was measured using the same setup as in case of the converter. The results of that comparison are presented in Table 3.

Table 3. Comparison of Measured Performance

Parameter	Converter	Transformer	Comment
s-s THD	*0.3 %*	*0.3 %*	$V_i = 1.2 V_{pp}$
dif. THD	*0.15 %*	*0.3 %*	"
max. freq.	*119 MHz*	*21 MHz*	$\Delta\varphi = 25^o$
min. freq.	*0 Hz*	*10 kHz*	"

The transformer introduces about the same amount of distortion as converter, but since the dominant component is 3-rd harmonic, no improvement for differential output is observed. In case of the converter, its distortion being

transformers resulting in better high-frequency, noise, and distortion performance, as well as savings in power and die area. Measurements show that for a *9 GHz* bipolar process with a power supply of *0 - 5 V*, *THD < 0.15%* for