Transactions Briefs

Highly Linear Voltage-Controlled CMOS Transconductors

Stanisław Szczepański, Adam Wyszyński, and Rolf Schaumann

Abstract—**A circuit technique for realizing voltage-tunable linear high-frequency CMOS transconductor cells is described which use two cross-coupled MOS or CMOS transistor pairs operating in saturation. The tuning capabilities with an adjustable CMOS voltage source are examined. Design trade-offs between linearity and bandwidth are discussed and a simple OTA example is simulated via SPICE. The simulation results show that the transconductance can be varied by a factor 8 and that, for a power supply ± 5V, the linearity error is less than 0.5% for an input voltage ± 3.0 V. A cutoff frequency of over 370 MHz is obtained.**

I. Introduction

MOS transconductors or voltage-to-current converter circuits are useful building blocks for the design of analog and mixed analog-digital signal processing systems. Such applications usually require very linear transconductance elements with a good high-frequency capability. In recent years, many advances for improving the linearity of MOS transconductor circuits were reported, e.g. [1]–[10]. Several CMOS operational transconductance amplifier (OTA) structures with good linearity were successfully implemented for applications in high-frequency filters.

In [1], a linear fully balanced CMOS OTA with a conventional source-coupled pair input stage was proposed in which the high-impedance tail current source is replaced by a voltage source. However, for this OTA, the output current is a linear function of excitation only if purely differential input signals are applied. This drawback is overcome by the approach presented in this paper. It uses two cross-coupled MOS transistor pairs, with one pair biased by an additional CMOS voltage source with low output impedance. The technique is extended to two cross-coupled CMOS transistor pairs which permit biasing by a simpler voltage source.

II. Voltage-Biased Source-Coupled Pair

First consider the source-coupled pair in Fig. 1 [1], [8]; it is identical to a conventional differential pair except that the common-source node is biased by a voltage rather than a current. Using the standard square-law model for perfectly matched transistors yields

$$I_{\Delta 1} = I_{d1} - I_{d2} = k_n(V_{gs1} + V_{gs2} - 2V_{Tn})(V_{gs1} - V_{gs2}) \quad (1)$$

where $k_n = k_{on}W/L = 0.5\mu C_{ox}W/L$ is the transconductance parameter, and μ, C_{ox}, W and L are the mobility, oxide capacitance per unit area, and channel width and length, respectively. V_{Tn} is the threshold voltage defined by

$$V_{Tn} = V_{T0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right) = V_{T0} + \Delta V_{Tn} \quad (2)$$

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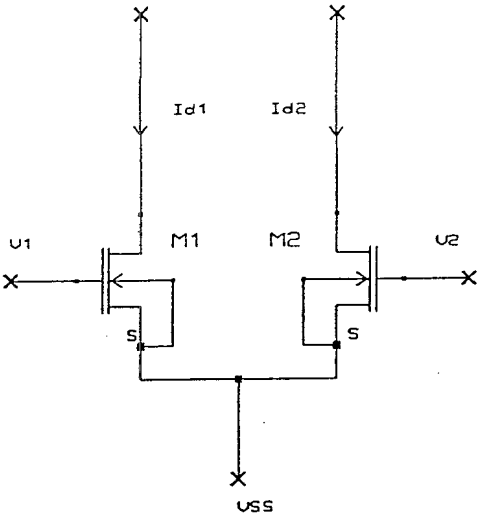

Fig. 1. Voltage-biased source-coupled pair.

where V_{BS} is the bulk-source voltage and V_{T0} the threshold voltage for $V_{BS} = 0$, γ the bulk threshold parameter, and ϕ the strong inversion surface potential. For the pair in Fig. 1, it is assumed that $V_{BS} = 0$, so that $V_{Tn} = V_{T0}$. The gate-source voltages defined in Fig. 1 are given by

$$V_{gs1} = V_1 - V_{SS} \quad (3a)$$

$$V_{gs2} = V_2 - V_{SS} \quad (3b)$$

where V_{SS} is the dc bias voltage. Defining the common-mode input level as

$$V_{CM1} = \frac{V_{gs1} + V_{gs2}}{2} \quad (4)$$

Equation (1) can be written in terms of V_{CM1} as follows:

$$I_{\Delta 1} = 2k_n(V_{CM1} - V_{Tn})V_d \quad (5)$$

where

$$V_d = V_{gs1} - V_{gs2} = V_1 - V_2 \quad (6)$$

is the differential input voltage.

It is seen from (1) and (5) that a linear transconductance of the MOS transistor pair in Fig. 1 can be obtained by insuring that the term $(V_{CM1} - V_{Tn})$ is constant, i.e., for purely differential input signals $(V_1 = -V_2)$. A circuit technique for overcoming this drawback is presented in the next sections.

III. Voltage-Adjustable Cross-Coupled Quad Cell

Consider two NMOS pairs (M_1, M_2) and (M_3, M_4) in the cross-coupled configuration shown in Fig. 2. Note, that this arrangement is obtained using the transistor pair in Fig. 1 in combination with a second pair (M_3, M_4) which is biased by the dc voltage source V_B. The transistors (M_1, M_2) and (M_3, M_4) are assumed to have their

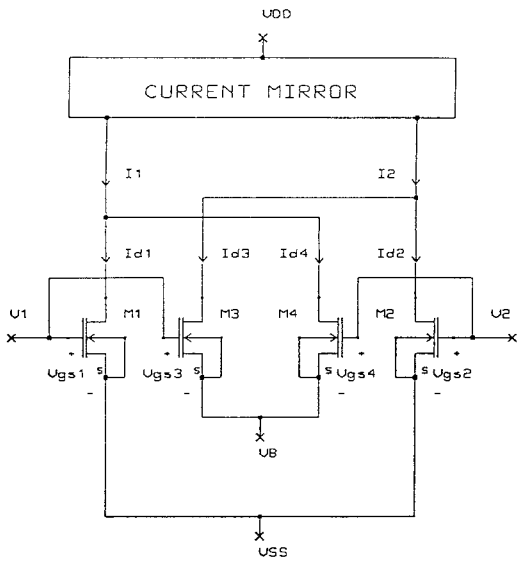

Fig. 2. Voltage-adjustable cross-coupled quad cell.

bulk connections tied to V_{SS} and V_B, respectively, so that no body effects occur.

Applying the standard square law model also for $M_3$and M_4 in the saturation region, the differential current $I_{\Delta 2}$ is obtained as

$$\begin{aligned} I_{\Delta 2} &= I_{d4} - I_{d3} \\ &= k_n(V_{gs3} + V_{gs4} - 2V_{Tn})(V_{gs4} - V_{gs3}) \\ &= 2k_n(V_{CM2} - V_{Tn})(-V_d) \end{aligned} \tag{7}$$

where the gate-source voltages V_{gs3} and V_{gs4} are given by

$$V_{gs3} = V_1 - V_B = V_1 - V_A - V_{SS} \tag{8a}$$

$$V_{gs4} = V_2 - V_B = V_2 - V_A - V_{SS} \tag{8b}$$

with V_A defined as

$$V_A = V_B - V_{SS} \tag{9}$$

Similar to (4), the term V_{CM2} in (7) represents the common-mode input of the second pair $(M3, M4)$:

$$V_{CM2} = \frac{V_{gs3} + V_{gs4}}{2} \tag{10}$$

and $V_d = V_{gs1} - V_{gs2} = V_{gs3} - V_{gs4} = V_1 - V_2$ is the differential input voltage of both pairs. From this analysis of the pairs (M_1, M_2) and (M_3, M_4) it follows that the total differential current I_{out} of the transconductor circuit in Fig. 2 is given by

$$I_{out} = I_1 - I_2 = I_{\Delta 1} + I_{\Delta 2} \tag{11}$$

which with (5) and (7) results in

$$I_{out} = 2k_nV_AV_d = g_mV_d \tag{12}$$

with the voltage V_A defined in (9). Note that g_m goes to zero for $V_A \rightarrow 0$, i.e., as V_B approaches V_{SS}. Thus, very small values of g_m for low-frequency applications can readily be realized.

Thus the proposed cross-coupled configuration exhibits a perfectly linear transconductance of value $g_m = 2k_nV_A$ which is tunable by varying the bias voltage V_A. Linearity is maintained as long as all devices remain on, that is the linear differential input range of the transconductor circuit in Fig. 2 is limited by

$$|V_d| < 2|V_B + V_{Tn}| \tag{13a}$$

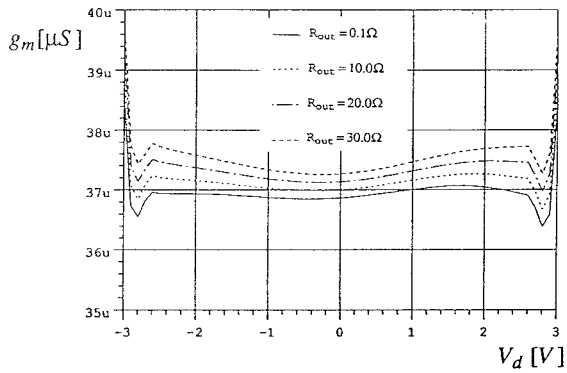

Fig. 3. Transconductance of the CMOS OTA in Fig. 8 as a function of the output resistance R_{out} of the adjustable voltage source V_B, for $V_B = -2.5$V.

or

$$|V_d| < 2|V_{SS} + V_{Tn}| \tag{13b}$$

whichever is smaller. Substituting $V_d \approx 0$ in (13a), the maximum control voltage $V_{B,\max}$ can be estimated as

$$|V_{B,\max}| > V_{Tn}. \tag{13c}$$

The above derivation assumed that both transistor pairs sit in their own wells so that body effects can be avoided. If this is not the case, all transistors normally have their bulk connections tied to V_{SS}. As a result, $V_{BS} \neq 0$ for transistors $M_3$and M_4, and including body effect in (7) leads to the linear voltage-to-current conversion

$$I^*_{out} = 2k_n(V_A + \Delta V_{Tn})V_d \tag{14}$$

where ΔV_{Tn} is the term which according to (2) approximates the dependence of the threshold voltage V_{Tn} on the bulk-source voltage V_{BS}. The linear range is now limited by (13), with V_{Tn} replaced by $V_{T0} + \Delta V_{Tn}$ in (13a, c).

From the above analysis, the principle of operation for the voltage-adjustable cross-coupled quad cell is apparent. Note, that the voltage source V_B must carry the current $I_B = I_{d3} + I_{d4}$ and that the voltage of node V_B must not vary with current; consequently, as as illustrated in Fig. 3, this circuit concept requires a voltage source V_B with extremely low output impedance to preserve high linearity of the transconductance. To alleviate the requirements for a voltage source the alternative circuit topology discussed in Section IV can be implemented that uses two CMOS double pairs. This approach is not sensitive to the output impedance of the voltage source because the source carries no current.

IV. Cross-Coupled CMOS Double Pairs

The topology is obtained by replacing each MOS transistor in the circuit in Fig. 2 with the CMOS pairs shown in Fig 4. From the simple quadratic MOS model, the gate-source voltage of the $n-$channel transistor is given by

$$V_{gsn} = \sqrt{\frac{I_d}{k_n}} + V_{Tn}$$

where V_{Tn} is the bulk-dependent threshold voltage given by (2); an analogous expression holds for the $p-$channel device. Then according to Fig. 4, the equivalent gate-source voltage $V_{gseq} = V_{gsn} + V_{gsp}$ for the CMOS pair is given [2] by

$$V_{gseq} = \sqrt{\frac{I_d}{k_{eff}}} + V_{T\Sigma} \tag{16}$$

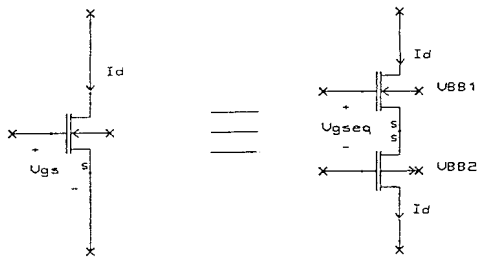

Fig. 4. Replacing single transistor by CMOS double pair.

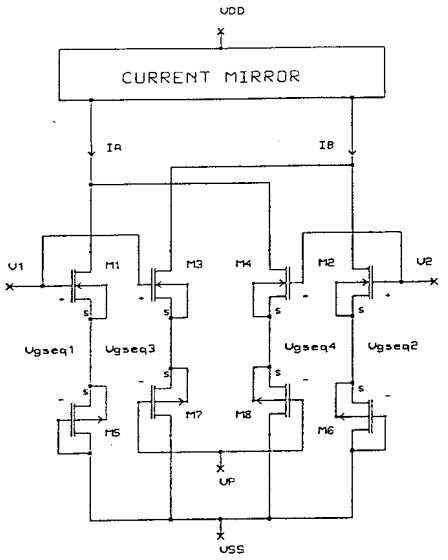

Fig. 5. Voltage-biased cross-coupled CMOS double pairs.

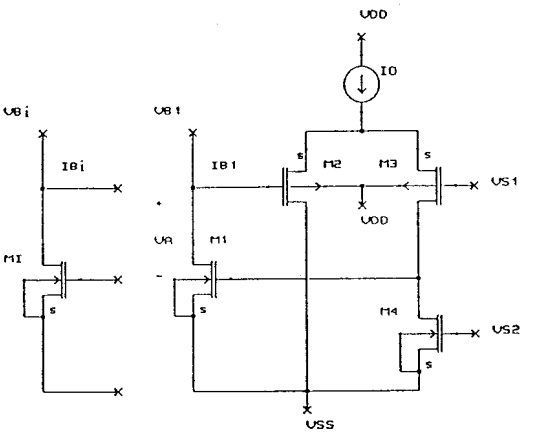

Fig. 6. Adjustable CMOS voltage source with output resistance $R_{out} < 10\Omega$.

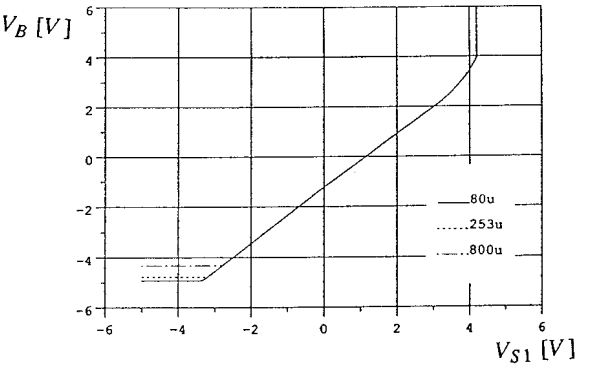

Fig. 7. Performance of the source in Fig. 6: $V_B = f(V_{S1})$ for $I_{B1} = 80\mu$A, 253μA, 800μA.

where

$$k_{eff} = \frac{k_n k_p}{(\sqrt{k_n} + \sqrt{k_p})^2} \tag{17}$$

and

$$V_{T\Sigma} = V_{Tn} + |V_{Tp}| \tag{18}$$

The undefined parameters have their usual meaning. Fig. 5 shows a complete circuit for a linear CMOS transconductor with all transistors biased in saturation, and with bulk connections assumed tied to their respective sources. Design guideliness for the case where body effects must be considered are given in [2]. Analogous to (12) the total differential output current $I_{out_{AB}} = I_A - I_B$ can be derived as

$$I_{out_{AB}} = 2k_{eff}(V_{CM_A} - V_{CM_B})V_d = 2k_{eff}V_C V_d = g_m V_d \tag{19}$$

where

$$V_{CM_A} = \frac{V_{gseq1} + V_{gseq2}}{2} \tag{20}$$

and

$$V_{CM_B} = \frac{V_{gseq3} + V_{gseq4}}{2} \tag{21}$$

are the common-mode input levels for the two CMOS double pairs biased by the voltage sources V_{SS} and V_P, respectively. The dc voltage V_C equals $(V_{CM_A} - V_{CM_B}) = V_P - V_{SS}$ and $V_d = V_{gseq1} - V_{gseq2} = V_{gseq3} - V_{gseq4} = V_1 - V_2$ is the differential input voltage as before. The linear range of the circuit in Fig. 5 is limited by (13) with V_{Tn} replaced by $V_{T\Sigma}$.

Note again that the transconductance $g_m = 2k_{eff}V_C$ is perfectly linear and may be varied electronically by adjusting the bias voltage $V_C = V_P - V_{SS}$. Moreover, as was mentioned, an important feature of the CMOS transconductor in Fig. 5 is that it can now accept a high-impedance adjustable voltage source V_P for tuning purposes because, being connected to the gates of M_7 and M_8, it carries no current. However, the simulation results given in Section VI show that the circuit in Fig. 5 has worse linearity than its NMOS counterpart in Fig. 2. Similarly, the linear range given by (13) shrinks, because of the increased threshold voltages $V_{T\Sigma}$ of a composite CMOS device given in (18). Additionally, for the same channel length, the frequency response of the CMOS transconductor in Fig. 5 is inferior to that of the NMOS circuit in Fig. 2, due to excess phase of PMOS devices. Bearing all these facts in mind, the reminding discussion will focus on the NMOS transconductor as the one giving better overall performance.

V. Adjustable CMOS Voltage Source

The transconductance of the circuit in Fig. 2 is assumed to be controlled by adjusting V_B. A suitable low-impedance CMOS voltage source is shown in Fig. 6. The high-gain negative feedback loop containing transistors M_1 through M_4 stabilizes the output voltage over a wide range of the current $I_{B1} = I_{d3} + I_{d4}$. The voltage source was designed with a nominal output resistance of less than 10Ω; its simulated performance for a range of a factor 10 in I_{B1} and for device parameters as given in Section VI is shown in Fig. 7. Note that the source in Fig. 6 can conveniently be used if many

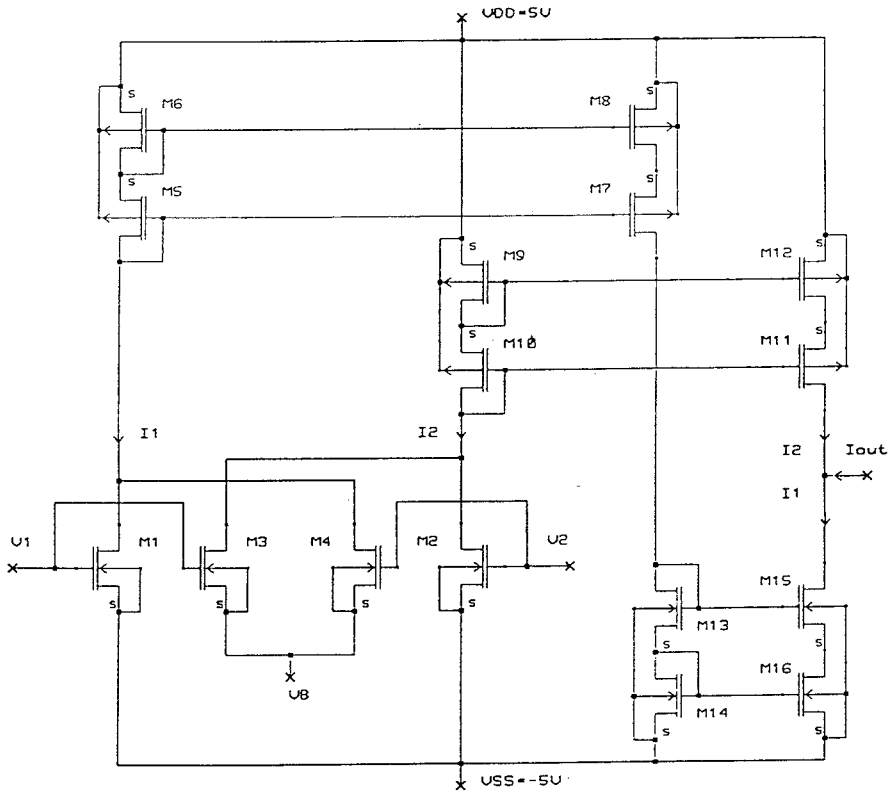

Fig. 8. Circuit diagram of a simple CMOS OTA with the gain adjustable linearly by the voltage V_B.

transconductances must be changed or tuned in a tracking fashion: as indicated in Fig. 6, one simply has to duplicate the branch with transistor M_1 an appropriate number of times.

VI. Simulation Results

The simple CMOS OTA in Fig. 8 was designed based on the circuit in Fig. 2 and simulated using SPICE with Level 2 models and 2μm MOSFET's with $V_{Tn} = 0.745$V, $V_{Tp} = -0.797$V, $k_{on} = 54.4\mu\text{A/V}^2$ and $k_{op} = 22.4\mu\text{A/V}^2$. The gate lengths are 3.8μm for transistors M_1 to M_4 and 2μm for M_5 to M_{16}. The gate widths are: $W_1 = W_2 = W_3 = W_4 = 3\mu$m, $W_5 = W_6 = \cdots = W_{12} = 30\mu$m and $W_{13} = W_{14} = W_{15} = W_{16} = 28\mu$m. The power supply is $V_{DD} = -V_{SS} = 5$V. In the voltage source in Fig. 6, $W_1 = 60\mu$m, $W_2 = W_3 = 36\mu$m, $W_4 = 12\mu$m, $L_1 = \cdots = L_4 = 6\mu$m, $V_{S2} = V_{SS}$, $I_0 = 100\mu$A and V_{S1} varies from -0.5V to -3.0V.

The simulated dc transfer curve $I_{out} = f(V_d)$ and the linearity error defined as

$$\epsilon = \frac{I_{out} - I_{out}(0) - g_m(0)V_d}{g_m(0)V_d} 100\% \qquad (22)$$

are shown in Fig. 9 for $V_{S1} = -2.5$V. The error is seen to be less than 0.5% in the differential input range ± 3V. Note that $I_{out}(0)$ was subtracted when determining ϵ in order to separate nonlinearities from the small dc offset. When V_{S1} is changed from -0.5V to -3V, the transconductance $g_m = dI_{out}/dV_d$ varies by a factor of 8, from 18μs to 144μs, with the linearity range limited by (13a) and (c) (see Fig. 10). For the cascode output stage in Fig. 8, the output impedance was found to be $|Z_{out}| > 1$ MΩ for $f \leq 15$MHz; the 3dB frequencies are between 330 MHz and 370 MHz over the whole tuning range (Fig. 11). If the transconductor in Fig. 8 had its input stage replaced by the CMOS circuit in Fig. 5, with all input devices having $L = 4\mu$m and $W_n = 8\mu$m for NMOS and $W_p = 12\mu$m for PMOS, the linearity

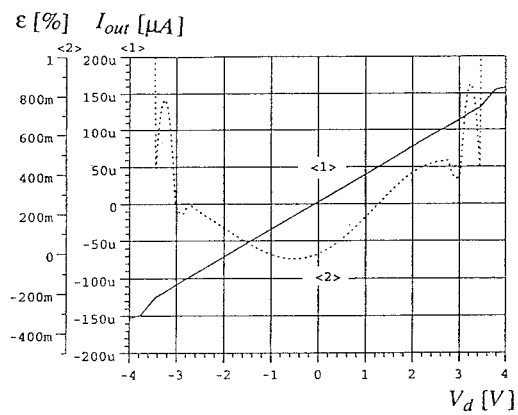

Fig. 9. Simulation results of the CMOS OTA in Fig. 8. <1> DC transfer curve of the output current I_{out}. <2> Linearity error defined by (22).

error would increase to 1%, for the differential input range ± 1.5V. At the same time, the simulated 3dB frequency is between 170 MHz and 210 MHz. Fig. 3 shows the transconductance of the simulated OTA when the output resistance R_{out} of the adjustable voltage source V_B is taken as a parameter. The simulation results indicate that the effect of R_{out} on the transconductance can be neglected for $R_{out} < 10\Omega$. Note that small geometries of the transistors are desirable for high-frequency performance. However, small length L and narrow channels result in such second-order effects as mobility degradation and finite output resistances (Early effect) of transistors and current mirrors, causing additional linearity errors. The distortion coming from these effects is mostly of even order so that the linearity error of the current transfer can be minimized by improving the

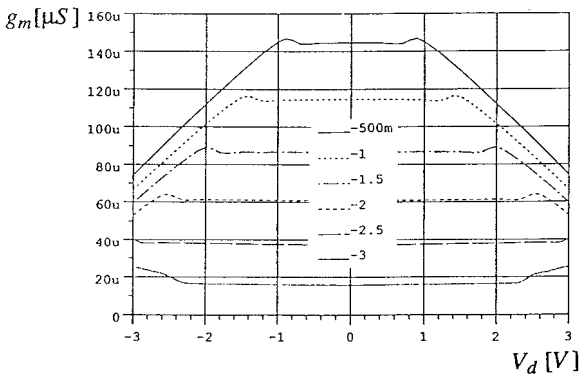

Fig. 10. Transconductance $g_m = dI_{out}/dV_d$ of the CMOS OTA in Fig. 8 as a function of V_d and V_{S1} as parameter. V_B realized by the source in Fig. 6.

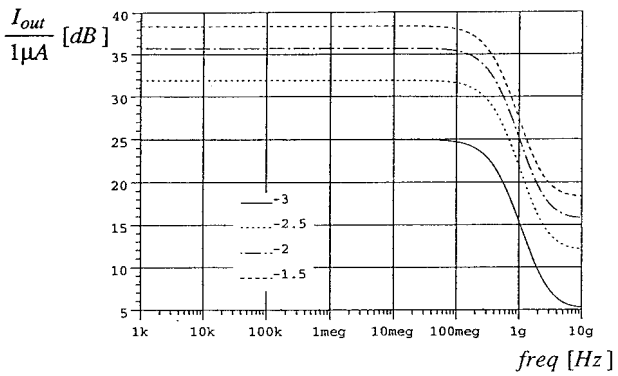

Fig. 11. Frequency response of the CMOS OTA in Fig. 8: I_{out} normalized to 1μA with V_{S1} as parameter.

OTA circuit symmetry. Note that the OTA structure in Fig. 8 is not symmetrical since the output is single-ended; better results can be obtained for fully differential structure. An example of such a circuit is given in [11]. It demonstrates improved linearity together with extended bandwidth.

VII. Conclusions

A circuit arrangement for high-frequency linear CMOS transconductance elements has been presented. The linearization technique is based on two cross-coupled MOS or CMOS double pairs operating in saturation. A large signal handling capability and high-frequency performance with 370-MHz cutoff frequency are obtained for the simulated CMOS OTA. A significant feature is the wide linear tunability of g_m by a voltage, permitting practical transconductance values as low as a fraction of 1μS. The simulation results obtained with the proposed concept indicate that this technique is suitable for many applications both in low-frequency and high-frequency analog interface circuits for VLSI.

References

[1] K. D. Peterson and R. L. Geiger, "A fully balanced CMOS OTA for high-frequency monolithic filters," *Proc. 29th Midwest Symp. Circuits and Systems,* pp. 208–211, 1987.

[2] C. S. Park and R. Schaumann, "A high-frequency CMOS linear transconductance element," *IEEE Trans. Circuits Syst.,* vol. CAS-33, pp. 1132–1138, Nov. 1986.

[3] V. Gopinathan, Y. Tsividis, K. Tan and R. Hester, "Design considerations for high-frequency continuous-time filters and implementations of an antialiasing filter for digital video," *IEEE J. Solid-State Circuits,* vol. SC-25, pp. 1368–1378, Dec. 1990.

[4] A. Nedungadi and T. R. Viswanathan, "Design of linear CMOS transconductance elements," *IEEE Trans. Circuits Syst.,* vol. CAS 31, pp. 831–834, Oct. 1984.

[5] K. Bult and H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristics of MOS transistors in saturation," *IEEE J. Solid-State Circuits,* vol. SC-22, pp 357-365, June 1987.

[6] R. R. Torrence, T. R. Viswanathan, and J. V. Hanson, "CMOS voltage-to-current transducers," *IEEE Trans. Circuits Syst.,* vol. CAS-32, pp. 1037-1104, Nov. 1985.

[7] Z. Czarnul and N. Fuji, "Highly-linear transconductor cell realized by double MOS transistor differential pairs," *Electron. Lett.,* vol. 26, pp. 1819–1821, Oct. 1990.

[8] C. Toumazou, F. L. Lidgey, and D. G. Haigh, *Analogue IC Design: The Current-Mode Approach.* London: Peter Peregrinus Ltd., 1990.

[9] A. Nedungadi and R. Geiger, "High-frequency voltage-controlled continuous-time low-pass filter using linearized CMOS intergrators," *Electron. Lett.,* vol. 22, pp. 729–737, June 1988.

[10] S. Szczepański, R. Schaumann, and P. Wu, "Linear transconductor based on cross coupled CMOS pairs," *Electron. Lett.,* vol. 27, pp. 783–785, Apr. 1991.

[11] A. Wyszyński and R. Schaumann, "VHF highly linear fully-balanced CMOS OTA," *Proc. IEEE Int. Symp. Circuits and Systems,* pp. 1156–1159, 1993.

A Frequency-Domain Technique for the Optimization of the Electrical Performance of High-Speed Multiconductor Transmission-Line Networks in VLSI Regimes

Tawfik Rahal-Arabi and Ricardo Suarez-Gartner

***Abstract*—This paper describes a new efficient technique for the optimization of the electrical performance of multiconductor transmission line and interconnect networks in VLSI regimes based on the minimization of an error function. The technique is particularly useful in the design of PCB interconnects as it significantly reduces the number of time and/or frequency-domain simulations required to ensure the functionality of a system design. To demonstrate the usefulness of the technique, several numerical examples have been solved and validated through time and frequency-domain simulations.**

I. Introduction

When the wavelength of the frequency of operation is very large compared to the physical size of the interconnect circuitry, the interconnects can be treated as mere connection points with no significant effect on the electrical performance of the system. With today's clock speeds and the continuing trend for faster digital circuits, the design of the electrical interconnect circuitry for optimum electrical performance is proving to be a major challenge and could be the bottleneck in an overall system design. Often an involved

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