

Q-Enhanced LC Bandpass Filters for Integrated Wireless Applications

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Abstract—*Q*-enhanced LC filter technology offers an alternative to the use of direct conversion techniques for implementing fully integrated receivers. Design and performance issues for QE LC filters are discussed and a fully integrated 850-MHz, two-pole, bandpass filter with an 18-MHz 3-dB bandwidth is reported. The prototype design is implemented in a standard 0.8- μ m CMOS process and achieves a rejection of over 50 dB at 100 MHz offset, an in-band dynamic range of 75 (90) dB when used in a system with a 1-MHz (30-kHz) final IF bandwidth, and a third-order intercept point that exceeds +25 dBm at an 80-MHz offset from the passband center.

Index Terms—Integrated receiver, *Q*-enhanced LC filter, RFIC, spiral inductor.

I. INTRODUCTION

A CENTRAL theme in radio frequency integrated circuit (RFIC) research and development in recent years has been the push toward a single-chip solution encompassing all circuitry from the antenna port to the information source/sink [1]–[11]. Unfortunately, due to a lack of suitable on-chip bandpass filtering technologies, such a device has proven difficult to realize.

Classic superheterodyne receivers, for example, require bandpass filters with narrow fractional bandwidths (on the order of 1% of center frequency) for preselection, image rejection, and final channel selection prior to demodulation. During the past decade, considerable research was directed at developing switched-capacitor and Gm-C based on-chip replacements for such requirements [12]–[33]. However, despite their continuous-time nature, achieving high operating frequencies with narrow bandwidths (high *Q*) proved difficult [29], and fundamental limitations on dynamic range at high *Q* values prevented their commercial application [34]–[36].

The problems encountered in this early research caused many researchers to abandon the superheterodyne architecture and turn to alternatives such as ultra-low IF and direct conversion designs [37]–[40]. Unfortunately, these architectures

present significant implementation problems. For example, concerns in the widely adopted direct conversion alternative include local oscillator (LO) leakage from the receiver, homodyning-induced dc offsets, $1/f$ noise associated with large baseband gains, significant area consumption by high-order baseband channel selection filters, and limitations on dynamic range from second-order as well as third-order intermodulation distortion [1], [38].

While many of the difficulties of implementing direct conversion architectures are being solved, the limitations on dynamic range are *fundamental* in direct conversion designs. By moving all channel select filtering to baseband, the low noise amplifier (LNA) and mixer circuits, which entail active devices with moderate combined gain to achieve reasonable noise figure performance, are left exposed to the full RF environment. Thus, strong signals *outside* as well as inside the desired service band can produce spurious responses and/or receiver desensitization, two of the most important problems facing high-performance radio design.

The only solutions to this problem of poor dynamic range performance in fully integrated devices are to either greatly increase the current consumption of the direct conversion design or to employ some preselect filtering. Thus, for fundamental reasons, the need for high-frequency, high-*Q* bandpass filtering cannot be completely eliminated. This fact, together with other advantages of classic heterodyning techniques in both the transmitter and receiver portion of radio circuits suggests that further research into on-chip bandpass filtering is still needed.

In this paper, the realization of integrated bandpass filters using on-chip spiral inductors and *Q*-enhancement techniques is investigated. This approach has been proposed by several researchers as a means to create narrow fractional bandwidth RF filters suitable for use in receiver front-end and first IF circuits [41]–[45]. The basic technology has been shown to be theoretically viable for such applications [34], but to-date, reported implementations in low-cost silicon IC technologies have demonstrated only moderate dynamic range performance (e.g., 50 dB) and have not realized practical high-order transfer function designs. The implementation reported here is a full fourth-order (two-pole) design operating at 850 MHz with a 2% (18 MHz) bandwidth. It achieves a 75 dB dynamic range when used in a cellular or PCS receiver with a nominal 1 MHz channel bandwidth and includes a companion oscillator for use in master–slave tuning. Increases in dynamic range for signals outside the filter passband are also demonstrated, and the performance of receivers using such filters is compared

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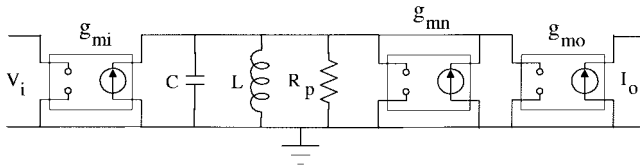


Fig. 1. Simplified Q -enhanced filter circuit-level diagram.

with receiver designs employing both traditional architectures and direct conversion (zero-IF) designs.

II. Q -ENHANCED LC FILTER DESIGN

A basic Q -enhanced filter design is illustrated in Fig. 1 [44]. This implementation is a simplified second-order (one-pole) bandpass topology built around a parallel-mode realization in which R_p represents the equivalent parallel loss resistance of the finite Q inductor and connected circuit at resonance, while transconductor g_{mn} implements a negative resistance designed to offset these losses. Transconductors g_{mi} and g_{mo} provide I/O buffering to form the complete second-order filter.

The effective quality factor Q_{eff} of this circuit, found from the net parallel resistance divided by the inductor reactance at the resonant frequency can be shown to be [44]

$$Q_{\text{eff}} = \frac{1}{1 - g_{mn}R_p} Q_o \quad (1)$$

where Q_o is the base Q of the resonant circuit (typically inductor limited). Hence, through suitable setting of g_{mn} , the effective Q can, in theory, be made as high as desired.

Realization of these circuits in modern RFIC processes is not difficult. However, the ultimate filter performance that can be achieved in terms of dynamic range versus power consumption and the need to tune the filter's center frequency and Q are important concerns [43], [46].

III. DYNAMIC RANGE OF Q -ENHANCED FILTERS

For a basic second-order resonator, the dynamic range (DR) achievable in a receiver employing a Q -enhanced bandpass filter can be expressed as [46], [47]

$$\text{DR} = \frac{P_{1\text{dB}}}{4kT(F+1)B_{\text{IF}}Q^2} Q_o^2 \quad (2)$$

where $P_{1\text{dB}}$ is the 1-dB compression point power in R_p , Q_o and Q are the resonant circuit quality factors before and after Q enhancement, respectively, B_{IF} is the final IF bandwidth of a receiver in which the filter is assumed to be used, F is a noise factor associated with g_{mn} and g_{mi} which assumes a value on the order of 1–2 [46], and kT is Boltzmann's constant times Kelvin temperature.

The dynamic range given by (2) for Q -enhanced LC filters, while limited by the active circuits and power consumption needed to achieve $P_{1\text{dB}}$, has been shown to be a factor of Q_o^2 higher than that in Gm-C filters operating at equivalent power consumptions and fractional bandwidths [34]. Thus, even with typical spiral inductor quality factors in the range of 3.5 at L-band frequencies, the dynamic range performance is improved by over 10 dB relative to purely active filter techniques, while

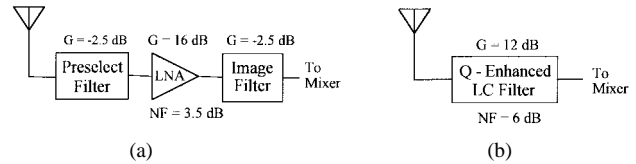


Fig. 2. Receiver front-end designs. (a) Traditional. (b) Q -enhanced filter.

if $Q_o = 10$ can be achieved, 20 dB of improvement can be obtained.

A. DR Within the Receiver System Context

Despite these advantages over fully active designs, (2) indicates that DR decreases rapidly as the filter bandwidth is narrowed through Q enhancement. Moreover, the use of active circuits necessarily means that power will be consumed. Thus, it may appear that the performance of receivers employing Q -enhanced filters would not compare favorably to existing receiver designs that incorporate off-chip passive devices. Fortunately however, this is not the case.

To illustrate this important point, two receiver front-end designs are shown in Fig. 2. Fig. 2(a) shows a traditional front-end incorporating off-chip preselect and image filters together with an integrated LNA. Although the passive filters of this design may have very high dynamic range by themselves, the LNA will limit the maximum signal levels allowed within the receiver's preselection passband, and thus the dynamic range of the system as a whole. For this case, the DR can be found from

$$\text{DR} = \frac{P_{1\text{dB}}}{kTF_{op}GB_{\text{IF}}} \quad (3)$$

where F_{op} and G are the operational noise figure and gain of the preselect filter + LNA combination, and $P_{1\text{dB}}$ is the compression point measured at the amplifier's output. Comparing this expression with (2) for the Q -enhanced filter of Fig. 2(b) (which includes gain as a byproduct of Q enhancement) reveals that similar dynamic range performance can be obtained if the Q enhancement is limited to

$$\frac{Q}{Q_o} \approx \sqrt{\frac{G}{3}} \quad (4)$$

assuming $F = 2$ in the filter, $F_{op} = 4$ in the preselector + LNA combination, and that $P_{1\text{dB}}$ is comparable in the two cases. For typical receivers, G may range from 12 to 25 dB (with the higher values applying when gain up through an active mixer is considered) implying Q enhancements from 2–10 should be possible without dynamic range penalties.

B. Protection from Out-of-Band Interferers

Equation (2) provides a useful upper bound on the dynamic range of a receiver employing a Q -enhanced filter. However, this bound applies only for the case where signals are within the filter passband. In the radio system context, the performance relative to interferers outside the service band is also important, and with a properly designed Q -enhanced preselect filter, the receiver's dynamic range relative to such signals is significantly increased.

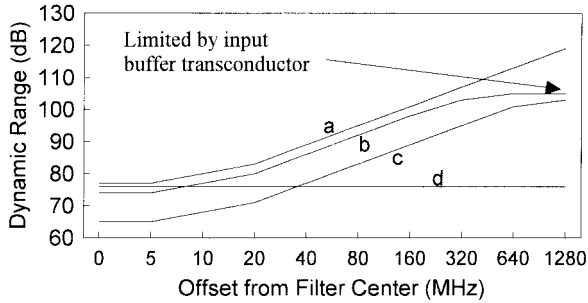


Fig. 3. Calculated dynamic range versus frequency for (a) traditional front-end design, (b) *Q*-enhanced *LC* filter-based design with $Q_o = 8$, (c) *Q*-enhanced design with $Q_o = 3$, and (d) direct conversion design.

To quantify this effect, let the input referred compression point of the filter be written as

$$P_{ci} = P_{co} - G(f) \quad (5)$$

where P_{ci} and P_{co} are the input and output compression points of the filter in dBm, and $G(f)$ is the filter gain in dB at frequency f . For a second-order (one-pole) bandpass design, $G(f)$ may be approximated for frequencies outside the passband as

$$G(f) \approx G_o - 20 \log \left| \frac{f - f_o}{B/2} \right| \quad (6)$$

where G_o is the midband gain, f_o is the center frequency, and B is the filter bandwidth. Combining (5) and (6) gives

$$P_{ci} \approx P_{co} - G_o + 20 \log \left| \frac{f - f_o}{B/2} \right|. \quad (7)$$

Noting that compression within the filter will occur first at the output due to the filter's gain, and that the output compression point is fixed by the bias point and power consumption of the resonator circuits, this equation suggests that input compression and dynamic range should improve at a rate of approximately 6 dB per octave away from the filter's edge.

C. Comparison with Traditional and Direct Conversion Designs

Based on these results, the dynamic range performance theoretically achievable with one-pole *Q*-enhanced filters using moderate inductor Q 's ($Q_o = 3$ and $Q_o = 8$) is shown in Fig. 3 and compared with the performance computed for a fully integrated direct conversion design without preselection and a traditional front-end design, both with the same gain (26 dB) and current consumption (5 mA) [46].

In both the *Q*-enhanced filter-based designs and traditional receiver, the dynamic range increases outside the preselect passband due to decreasing system gain at large offsets. For a *fully integrated* direct conversion receiver, however, dynamic range outside the service band remains at its in-band value since no preselect filter is present.¹

¹Full integration assumes that no discrete antenna/duplex filtering is used—a situation which becomes possible in receive-only products and in TDD or TDMA transceivers.

IV. FILTER TUNING

All high-*Q* active filters, including *Q*-enhanced designs, are known to suffer from problems with frequency/*Q* manufacturing tolerances and temperature drift. Although these problems are reduced in a *Q*-enhanced *LC* filter due to the natural stability of the *LC* resonators used, some form of real-time tuning is still needed for *Q* enhancements of about five or above [44].

The simplest approach to tuning is to employ a master–slave technique adapted from the design of Gm-C filters [48]. The viability of master–slave tuning in *Q*-enhanced *LC* filter design has been investigated in earlier development work [42], [44] and is not addressed further in this paper. A detailed analysis of *Q*-enhanced filter manufacturing tolerances and temperature sensitivities and of alternatives to the master–slave technique can be found in [44] and [47], respectively.

V. EXPERIMENTAL FILTER DESIGN

To investigate the performance of higher order *Q*-enhanced filters in low-cost silicon technologies at *L*-band frequencies, an experimental 850-MHz *Q*-enhanced *LC* filter was designed and fabricated in a standard 0.8- μm CMOS process. A fourth-order (two-pole) design with a bandwidth of approximately 20 MHz was desired to allow the filter to work in a traditional superheterodyne architecture and provide good image rejection when the received signal is downconverted to an intermediate frequency (IF) in the range of 60 MHz. The in-band dynamic range target was 75 dB for a system employing a nominal 1-MHz bandwidth. Although tuning of the filter was not part of the development effort, an associated oscillator was provided within the design to assess phase noise performance and oscillator-to-filter coupling effects.

A. Chip Architecture

The experimental chip architecture is shown in Fig. 4. Three fully differential, on-chip *LC* resonators are constructed around three 500- μm 8-turn center-tapped spiral inductors. The center-tapped geometry employs two interwound spirals constructed in the upper metal layer, together with a patterned poly ground shield similar to that discussed in [49]. The use of interwound spirals in place of two separate spirals increases the self-resonant frequency and conserves space on the die [50], while the ground shield minimizes losses that would otherwise occur from currents conducted through metal-to-substrate capacitance [51].

Two of the three resonators are identical and form the core of a coupled-resonator filter. The remaining resonator is configured to operate as the on-chip oscillator at a fixed 60-MHz offset from the filter passband. This offset prevents excessive magnetic coupling of the large amplitude oscillator signal into the filter and is designed to allow the oscillator to double as an LO for downconversion to a 60-MHz IF while fulfilling its primary role as a tuning reference in a master–slave filter tuning architecture.

Input–output transconductors implemented with standard differential pairs provide buffering of the resonator circuits to external test equipment used in the experimental chip

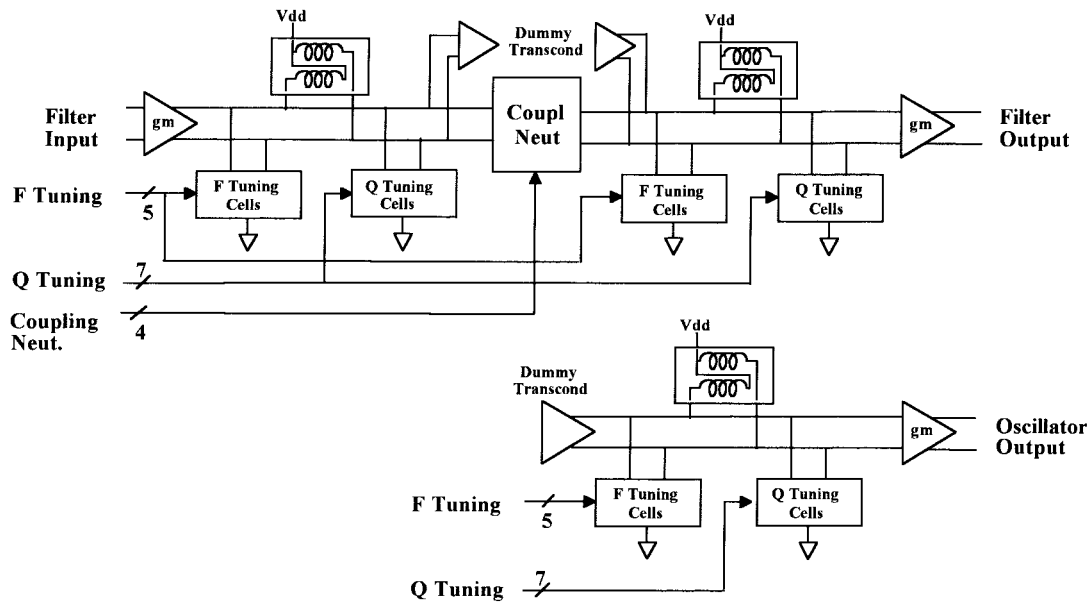


Fig. 4. Chip architecture.

evaluation. Internal dummy transconductors shown in Fig. 4 guarantee matching between resonators, simplifying tuning.

To yield a fourth-order response with the desired bandwidth, the filter inductors are magnetically coupled through suitable placement on the die. With ideal inductors, magnetic coupling between filter resonators results in an induced voltage in one resonator which is in phase quadrature with the current in the opposite inductor or, equivalently, an induced current in one resonator which is in quadrature with the voltage in the opposite resonator's voltage waveform. These phase relationships are necessary for a flat passband response. However, with on-chip spiral inductors, inductor currents and voltages are not in quadrature due to the resistive losses present, and significant passband asymmetries result [44]. A coupling neutralization circuit which injects signal current into one resonator proportional to the signal voltage in the opposite resonator is placed between the two resonators in this design to cancel the undesired effects of the in-phase component of the inductor's I/V relationship. Digital control allows a simple one-time trim of passband ripple to better than 2 dB.

Filter and oscillator frequencies are set through 5-bit digital control words. Use of digital tuning allows high- Q tuning capacitors to be implemented, making resonator starting quality factor (before Q enhancement) primarily dependent on inductor Q . This maximization of starting Q is essential to achieving good dynamic range at acceptable power consumption (Section III) and minimizes frequency drift with temperature [44]. Within each LC resonator, approximately 80% of the total C value originates from the inductor's turn-to-substrate capacitance, with the remaining C contributed by connected I/O buffers, Q tuning cells, and frequency tuning cells. Thus, resonator frequency is largely determined by capacitance within the inductor, allowing the tuning range to be relatively small in a process with tight oxide thickness tolerances. The prototype design provides a range of 60 MHz with a resolution of approximately 1.8 MHz (10% of the nominal filter bandwidth).

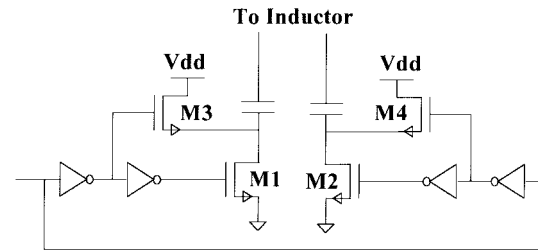
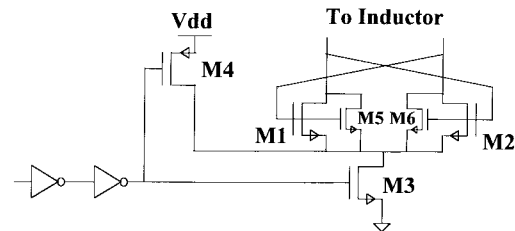


Fig. 5. Frequency tuning cell.

Fig. 6. Q tuning cell.

Tuning of filter Q is performed through a 7-bit digital control word, yielding the necessary range to compensate for variations in filter starting Q while providing a resolution of 15% of the nominal enhanced Q of 70. This Q resolution maps to a resolution of better than 20% in filter bandwidth.

B. Frequency Tuning Circuits

Frequency tuning is performed by switching grounded capacitors in and out of the resonator circuits using suitable arrays of the core circuit of Fig. 5. Metal-metal capacitors connected to the inductor are switched to ground on demand through M1 and M2 which are sized to provide good capacitor Q when on. When M1, M2 are off, minimum geometry FET's M3 and M4 pull the drain of the larger M1, M2 transistors to $V_{dd} - V_{th}$, reducing M1, M2 parasitic capacitance and improving linearity. On-off capacitance ratio for the complete

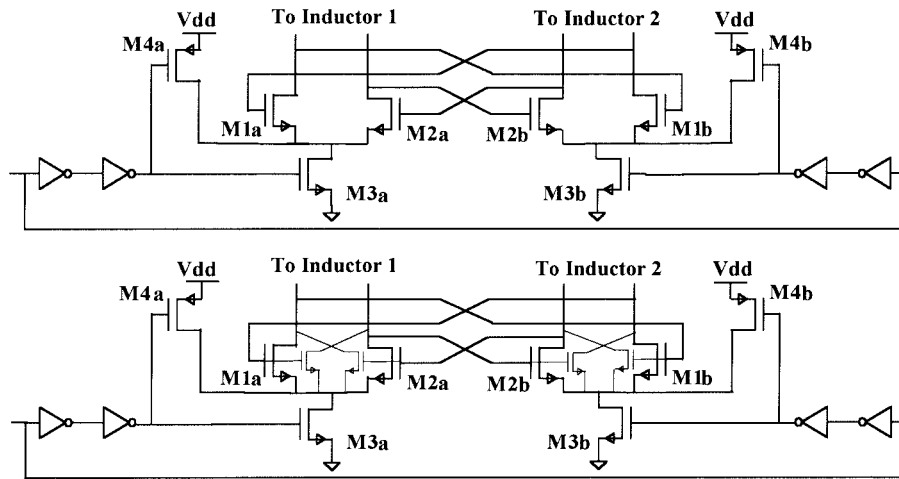


Fig. 7. Coupling neutralization circuits.

circuit is approximately 2 : 1, and the calculated quality factor of the capacitances is approximately 20 when on and ten when off. This capacitor Q is found to have negligible effect on the resonator’s starting Q when the relatively small fraction of total resonator capacitance contributed by the tuning circuits is taken into account.

C. Q Tuning Circuits

The circuit used for Q tuning is shown in Fig. 6. The circuit implements a negative resistance used to offset losses within the resonators, raising the effective resonator Q . The core circuit consists of cross-coupled transconductor M1, M2 which provides the negative resistance function, switch M3 to enable or disable the circuit, and pullup M4 to guarantee that when disabled, the circuit remains off in the presence of large signal swings on the inductor. Transistors M5, M6 are used in the LSB’s to decrease the effective transconductances below that possible with minimum geometry FET’s. The MSB is implemented with 16 copies of the circuit, with transistors M5 and M6 deleted. Lesser significant bits are composed of eight, four, two, and one copy with M5, M6 deleted, while the two least significant bits use a single copy with M5, M6 included.

D. Coupling Neutralization Circuits

Four bits of neutralization control are provided to allow for uncertainty in the inductor’s I/V nonideality. Two of the four bits drive the circuits shown in Fig. 7, while the remaining two bits drive a copy of these circuits in which the connection to one resonator’s inductor is reversed—a configuration designed to minimize capacitive coupling between the two resonator cores. As in the Q tuning cells, the LSB in each copy of this circuit is implemented with additional FET’s designed to lower the differential transconductance below that possible with minimum channel length devices.

VI. CIRCUIT LAYOUT

The filter and oscillator circuits described above were implemented in a standard 0.8- μm 1-poly, 3-metal, CMOS process. A photograph of the chip layout appears in Fig. 8. The filter

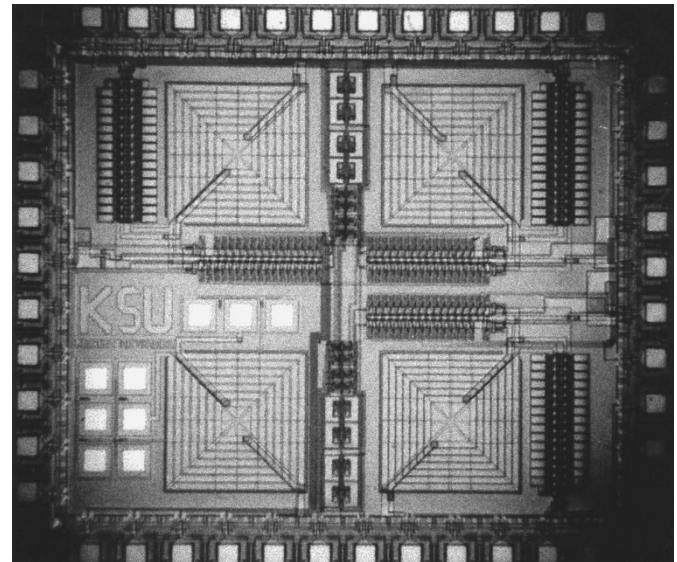


Fig. 8. Die photograph.

resonators are located in the upper half of the die, while the associated oscillator is positioned at the lower right. The additional inductor in the lower left is part of a test structure for measuring the inductor performance.

VII. MEASURED RESULTS

The filter response (S_{21}) measured from the input to final output using external 4:1 impedance baluns is shown in Fig. 9. For this measurement, the frequency controls were set to mid-range and the desired selectivity Q was achieved through manual setting of the Q controls. Coupling neutralization was then adjusted to provide a flat passband response. As shown, the filter achieves the desired 20-MHz bandwidth and the ultimate rejection exceeds 50 dB at 200 MHz offset from center.

The effect of the frequency tuning controls on the filter’s response is shown in Fig. 10 with the horizontal scale reduced to 20 MHz per division. The left, middle, and right curves illustrate the responses for tuning control codes of 11111,

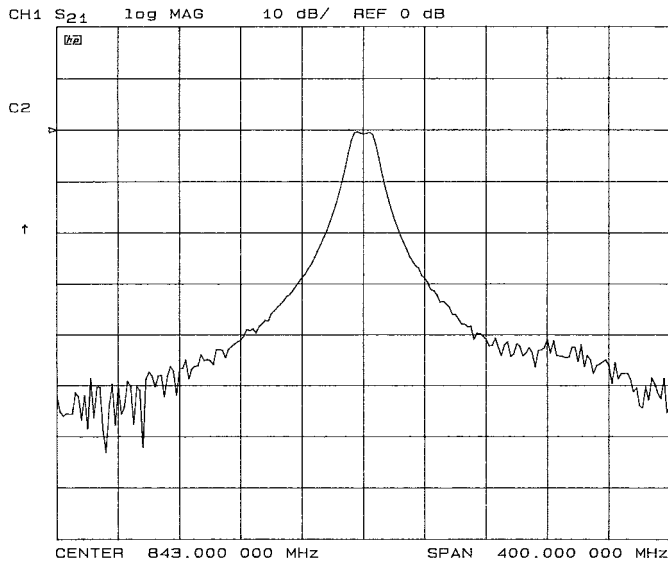


Fig. 9. Measured filter response: 843 MHz center, 10 dB/div vertical, 40 MHz/div horizontal.

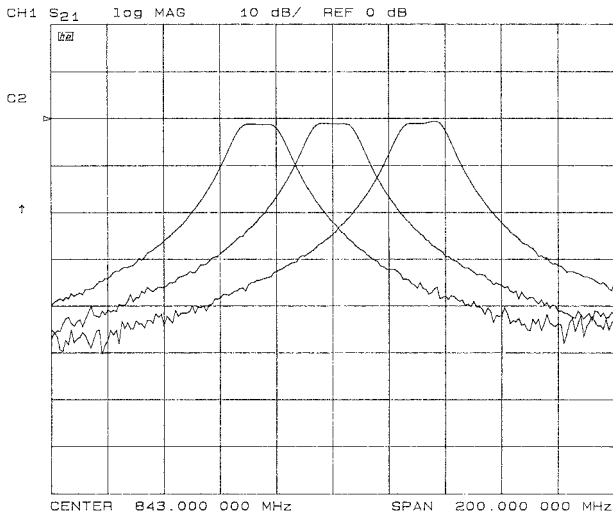


Fig. 10. Filter response versus frequency tuning: 10 dB/div vertical, 20 MHz/div horizontal.

10000, and 00000, respectively. These curves were obtained by manually readjusting Q control settings as needed to obtain a flat passband response with the nominal gain in each case. Coupling neutralization controls were left at a constant setting for all curves, however, to assess the need for real-time neutralization control. The passband ripple variation of less than 1 dB shows that a one-time trim of neutralization is sufficient.

The effect of Q tuning controls on the filter's transfer function is shown in Fig. 11. The bottom trace shows the response with all Q controls off. This trace represents the dynamic range limits of the network analyzer used. The remaining curves show increasing response with increasing Q control settings, with the top five curves representing increases of the Q control code by one LSB per step.

The effect of the coupling neutralization controls on filter response is shown in Fig. 12. The three curves represent

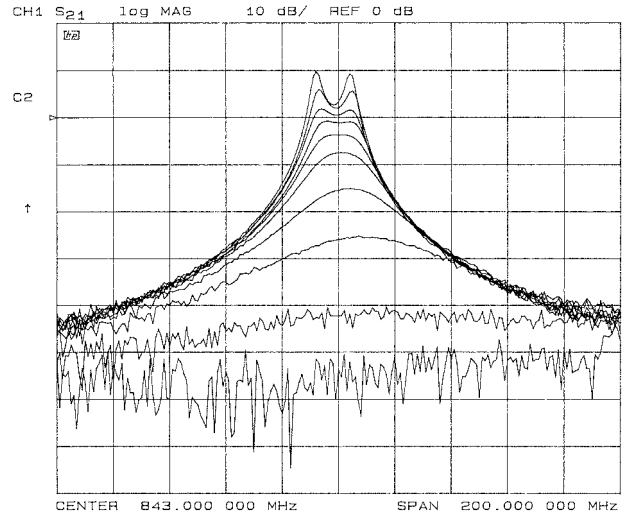


Fig. 11. Filter response versus Q tuning: 10 dB/div vertical, 20 MHz/div horizontal.

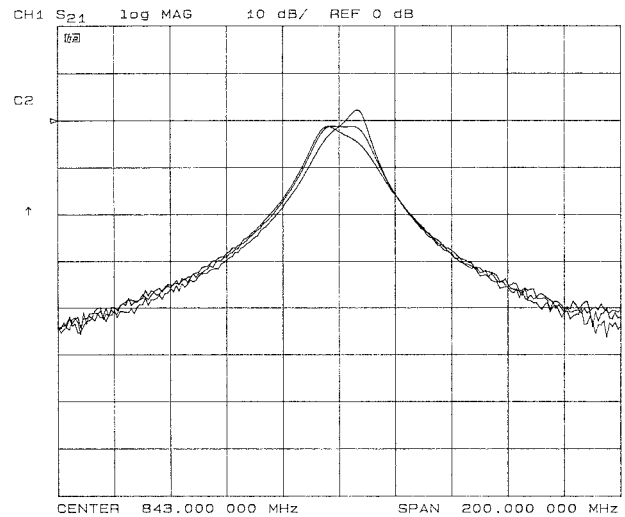


Fig. 12. Filter response versus coupling neutralization tuning: 10 dB/div vertical, 20 MHz/div horizontal.

the results for no neutralization (curve with highest peak), full neutralization (curve with opposite tilt), and optimal neutralization (flat passband).

A. Temperature Effects

The effects of temperature on frequency, Q , and coupling neutralization settings can be seen in Fig. 13. The right-most curve shows the response at approximately 5 °C with Q controls set to achieve a flat response. The lower curve represents the response after warming the chip to approximately 25 °C without readjustments. Q controls were then readjusted to achieve the flat passband response shown in the left curve.

The variation in frequency observed is well within the tuning range of the filter, even when a larger temperature range is considered, confirming the inherent stability of LC circuits seen in previous work on one-pole designs at lower frequencies [44]. Nevertheless, the need for real-time tuning of Q and frequency using a master-slave or other tuning system

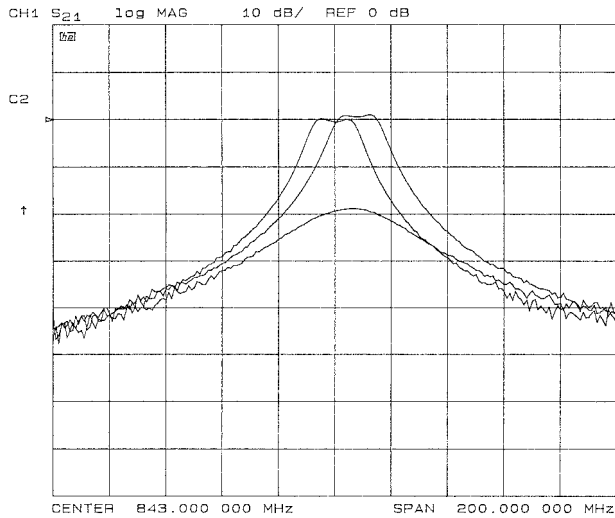


Fig. 13. Filter responses versus temperature (see text): 10 dB/div vertical, 20 MHz/div horizontal.

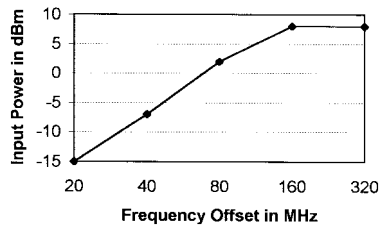


Fig. 14. Input 1-dB compression point versus frequency offset from pass-band center.

architecture is clearly seen. Coupling neutralization controls were left unchanged for all curves, indicating low sensitivity of neutralization to temperature and confirming the viability of employing a simple one-time neutralization trim.

B. Dynamic Range

The in-band dynamic range of the filter was measured as the ratio of the 1-dB compression output power (−18 dBm) to noise output power of −93 dBm measured in a 1-MHz resolution bandwidth, yielding 75 dB. When translated to a system with a 30-kHz channel bandwidth, the noise floor falls to −108 dBm, and the dynamic range approaches 90 dB.

To assess the filter’s out-of-band dynamic range performance, both compression and third-order distortion measurements were made. To measure compression, a signal at −30 dBm was placed within the filter passband and an interfering signal was introduced at various frequency offsets. The interfering signal power was increased until the in-band signal’s output level fell from its nominal value by 1 dB. The results of these measurements are shown in Fig. 14.

Based on the analysis in Section III, an improvement of approximately 6 dB/octave of frequency offset can be expected. Although the analysis was performed for the case of a one-pole filter, the results were expected to apply in the case of a two-pole design as well since the onset of compression should occur in the first resonator, whose response rolloff is approximately one-pole. The measured results shown in

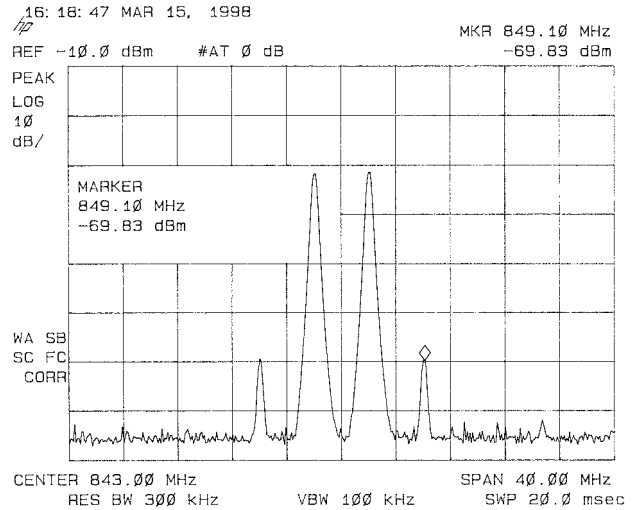


Fig. 15. In-band third-order intercept measurement.

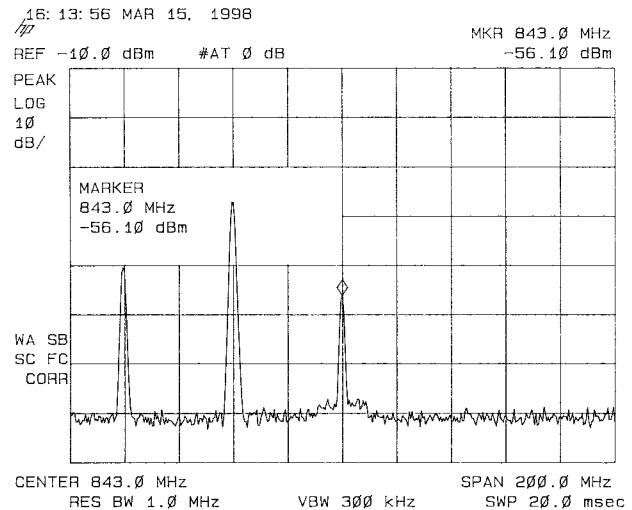


Fig. 16. Out-of-band third-order intercept measurement with interferer input power level of −10 dBm.

Fig. 14 indicate slightly better performance with an increase on the order of 8–9 dB/octave seen up to a maximum of 30 dB improvement over the midband value. The flattening of the curve at large offsets is attributed to the onset of saturation in the input buffer transistor at a value corresponding to roughly 1.6 V peak at 200 Ω (the value of the source impedance after transformation in the 4 : 1 impedance balun).

Third-order intercept measurements were performed for the case of in-band signals and for interferers at frequency offsets of 40 and 80 MHz. The measurements are shown in Figs. 15 and 16. For the in-band case, two signals at −30 dBm were introduced into the filter with a spacing of 4 MHz to keep third-order products well within the filter passband. The products are seen to be approximately 40 dB below the two tone signals applied, implying an intercept point of approximately 20 dB above the two-tone signals, or −11 dBm.

In the out-of-band case, two signals were placed at offsets of Δ*f* and 2Δ*f* and increased until a significant third-order product appeared within the filter passband. In Fig. 16, the input signals are 40 and 80 MHz from the filter center so

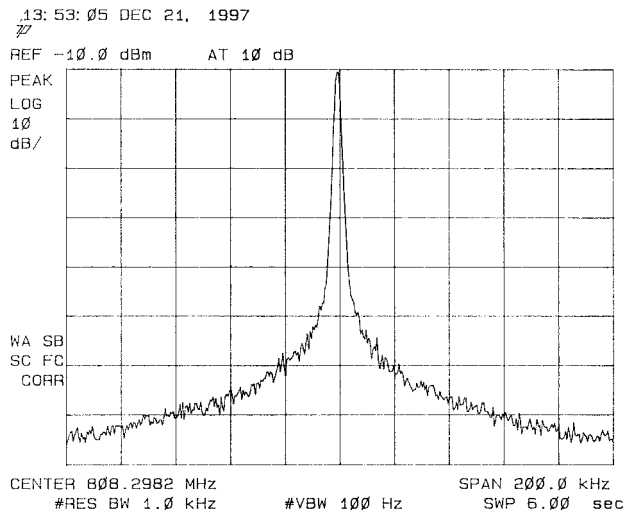


Fig. 17. Measured oscillator noise: 1 kHz RBW, 20 kHz/div.

that the third-order product falls in-band. The input power level for each interferer was set to -10 dBm, and the output product is found to be -56 dBm, implying an intercept point of $+13$ dBm. Similar measurements were made for signals at 80 and 160 MHz offset and resulted in an intercept point of $> +25$ dBm. In all cases, the filter gain was observed to decrease and the bandwidth broadened when sufficiently large signals were introduced. This behavior implies that the filter remains stable and does not enter oscillation, despite the large Q enhancements used.

C. Oscillator Performance

As a final test, measurements were made on the oscillator circuit included in the design to assess its phase noise, tracking with filter frequency, and its feedthrough into the filter.

The oscillator phase noise spectrum is shown in Fig. 17. Phase noise performance is -85 dBc/Hz at 10 kHz offset and -105 dBc/Hz at 100 kHz offset. The measured offset of the oscillator frequency from filter passband center was found to be 62 MHz and varied by less than 2 MHz for a 20 °C temperature change. Feedthrough from the oscillator into the filter was 20 dB below 1 dB compression in the second (output) resonator.

D. Performance Summary

A summary of measured performance is provided in Table I for both the filter and oscillator circuits.

VIII. CONCLUSIONS AND FUTURE DIRECTIONS

The prototype design described in this paper implements a practical two-pole response and achieves dynamic range performance exceeding that of previous *single-pole* designs by more than 20 dB. The filter provides a narrow bandwidth of approximately 20 MHz at 850 MHz, a flat passband response, and an ultimate rejection exceeding 50 dB. An in-band dynamic range of 75 dB increases to over 100 dB at 160 MHz offset due to attenuation of out-of-band signals, and

TABLE I
MEASURED PERFORMANCE

Parameter	Value
Transfer function type	2-pole coupled resonator
Center frequency	840 MHz
Nominal	816 MHz / 875 MHz
Min/max	
3 dB bandwidth	18 MHz
Midband gain	0 dB
Passband ripple	< 2 dB
Ultimate rejection	> 50 dB
Input 1 dB compression (in-band)	-18 dBm
Input referenced noise floor	
1 MHz final IF bandwidth	-93 dBm
30 kHz final IF bandwidth	-108 dBm
In-band 1 dB compression dynamic range	
1 MHz final IF bandwidth	75 dB
30 kHz final IF bandwidth	90 dB
Dynamic range at 160 MHz offset	
1 MHz final IF bandwidth	> 100 dB
30 kHz final IF bandwidth	> 115 dB
Input third order intercept	
In-band	-10 dBm
40 MHz offset from center	+13 dBm
80 MHz offset from center	$> +25$ dBm
Oscillator offset from filter	62 MHz
Oscillator phase noise	
10 kHz offset	-85 dBc/Hz
100 kHz offset	-105 dBc/Hz
Supply voltage	2.7 - 3.0 V
Supply current (at 2.7 V)	
Filter only	77 mA
Filter plus oscillator	114 mA
Die area (excluding pads)	2 mm ²

the ultimate out-of-band input referenced third-order intercept point exceeds $+25$ dBm.

Increasing compression and intercept points with frequency offset make the technology especially attractive for fully integrated receiver applications in which strong out-of-band interferers are expected in the environment and provides a significant advantage over fully integrated direct conversion receiver designs in which preselect filtering is omitted. However, it should be noted that the power consumption of the reported design currently restricts applications to base/mobile systems, and noise figure performance has not yet been optimized.

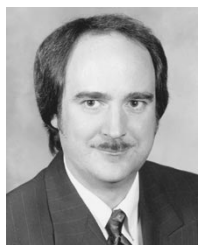
The relatively high current consumption shown in Table I was needed in the experimental chip to achieve the 75-dB dynamic range target specification in a digital CMOS process where inductor Q is less than three. In a more "inductor friendly" process where $Q_o = 8$ could be achieved [51], [52], or in applications where wider fractional bandwidths (lower Q enhancements) are acceptable, (2) suggests that current consumption could be reduced by as much as an order of magnitude without sacrifices in dynamic range performance.

The relatively high input referred noise floor observed is due to low gains used within the input and output buffer transconductors to achieve a desired 0-dB overall filter gain in this development effort. With increases in the input buffer gain, both the noise floor and compression/intercept points should decrease at comparable rates, so that dynamic range performance remains relatively constant, at least down to a noise figure of 6 dB [47]. At the same time, the ultimate

input-referred intercept point at large frequency offsets, which depends only on the input buffer bias voltage and source impedance level, should remain unchanged from the values measured here, maintaining the critical out-of-band performance advantages offered by this emerging technology.

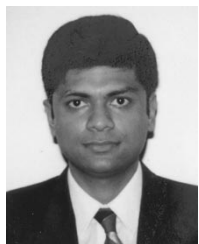
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